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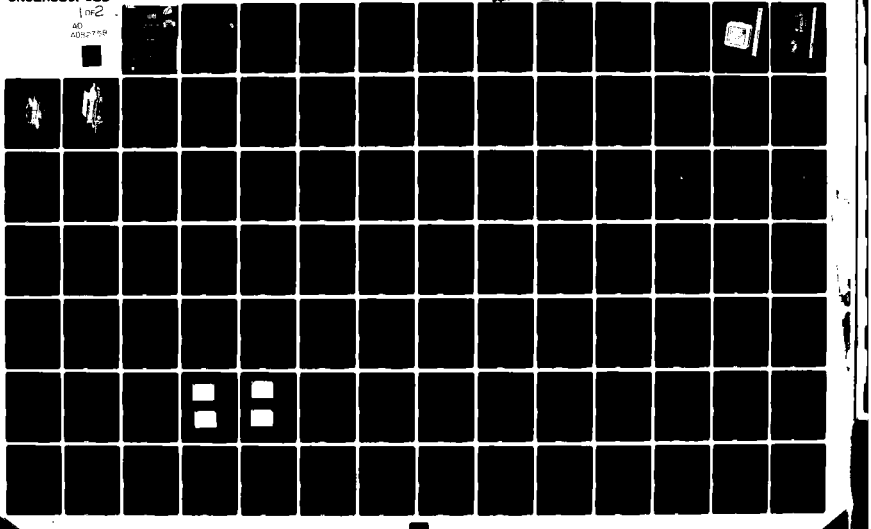

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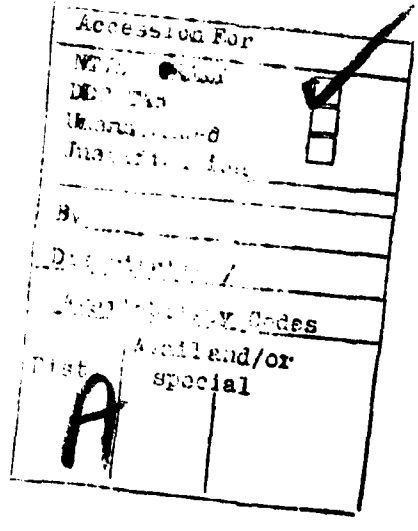
Block No. 20 ABSTRACT

A solid state power controller has been designed in four ratings to switch 28vDC power to selected loads upon remote command. The four ratings trip out at currents of 10, 5, 2 and 1/2 amps. The design allows for wide variations in load and supply voltage and will not trip out on short load transients of up to 1000% of rated load current. In case of failure of the controller circuitry, an internal fuse protects the load from excessive current. The control current which operates the controller also provides a sensing function so that the state of the controller can be determined remotely. The controllers are designed to operate over a case temperature range of -54°C to 120°C. A quantity of 100 units have been fabricated, tested, and supplied to the Navy.



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1.0 INTRODUCTION

The Final Report for the DC Controller program was prepared for the Naval Air Development Center under Contract #N62269-77-C-0413. The text describes the circuit operation, physical construction, assembly techniques and test procedures used in the manufacturing of one hundred power controllers. The controllers delivered operate from a nominal 28V supply and are rated for either 10A, 5A, 2A or 1/2A output load. These units were designed to comply with the requirements of Specification No. NADC-30-TS-7602 dated 27 April 1976.

This report describes the electrical design in Section 2, the physical design in Section 3, and the manufacturing process in Section 4. Appendix A is the parts list.

2.0 CIRCUIT DESIGN AND OPERATION

2.1 General Description

The electrical design of the DC power controller was divided into three subcircuits each of which was incorporated as a thick-film hybrid. As shown in Figure 1 the Power, Logic and Amplifier hybrids provide all switching, sensing, control and voltage regulator functions internal to the controller. Since the internal sense and control functions are not dependent on the power rating of the controller module, the logic and amplifier hybrids are identical for all controllers produced. The power hybrid is constructed with a maximum of four parallel power switching stages for a 10A rated unit. For 5A, 2A or 1/2A rated controllers, the same ceramic substrate was used for the power deck construction but with fewer of the parallel switching sections implemented. By using this technique, effectively, only one power hybrid had to be developed and the physical design task was reduced to developing only one controller type. Figure 2a shows the unit with the cover on, and Figure 2b, 2c and 2d show the unit with the cover off.

2.2 Subcircuit Design and Operation

The three subcircuits of each controller were partitioned so that the interconnection between the hybrids would be minimized as shown in Figure 1. The amplifier and logic hybrids were joined back to back in a sandwich arrangement with three opto-couplers mounted on the side to form the control subassembly. The power hybrid was soldered onto the steel header and a discrete diode was added internal to the terminal posts to form the power subassembly. The interconnections between the two subassemblies were then reduced to five interface wires in addition to four of the five terminal posts brought in from the outside of the controller.

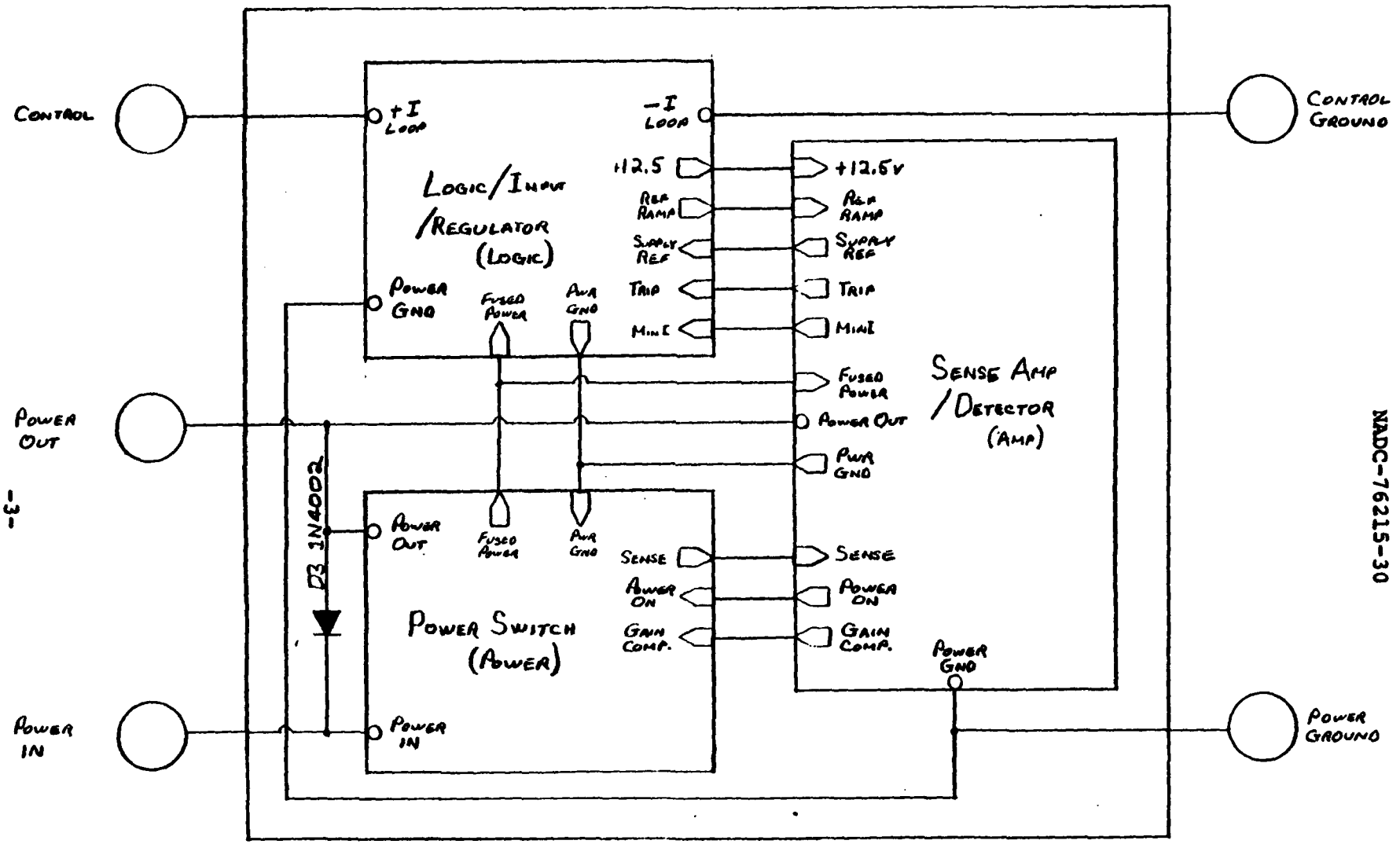


Fig. 1

General Block Diagram

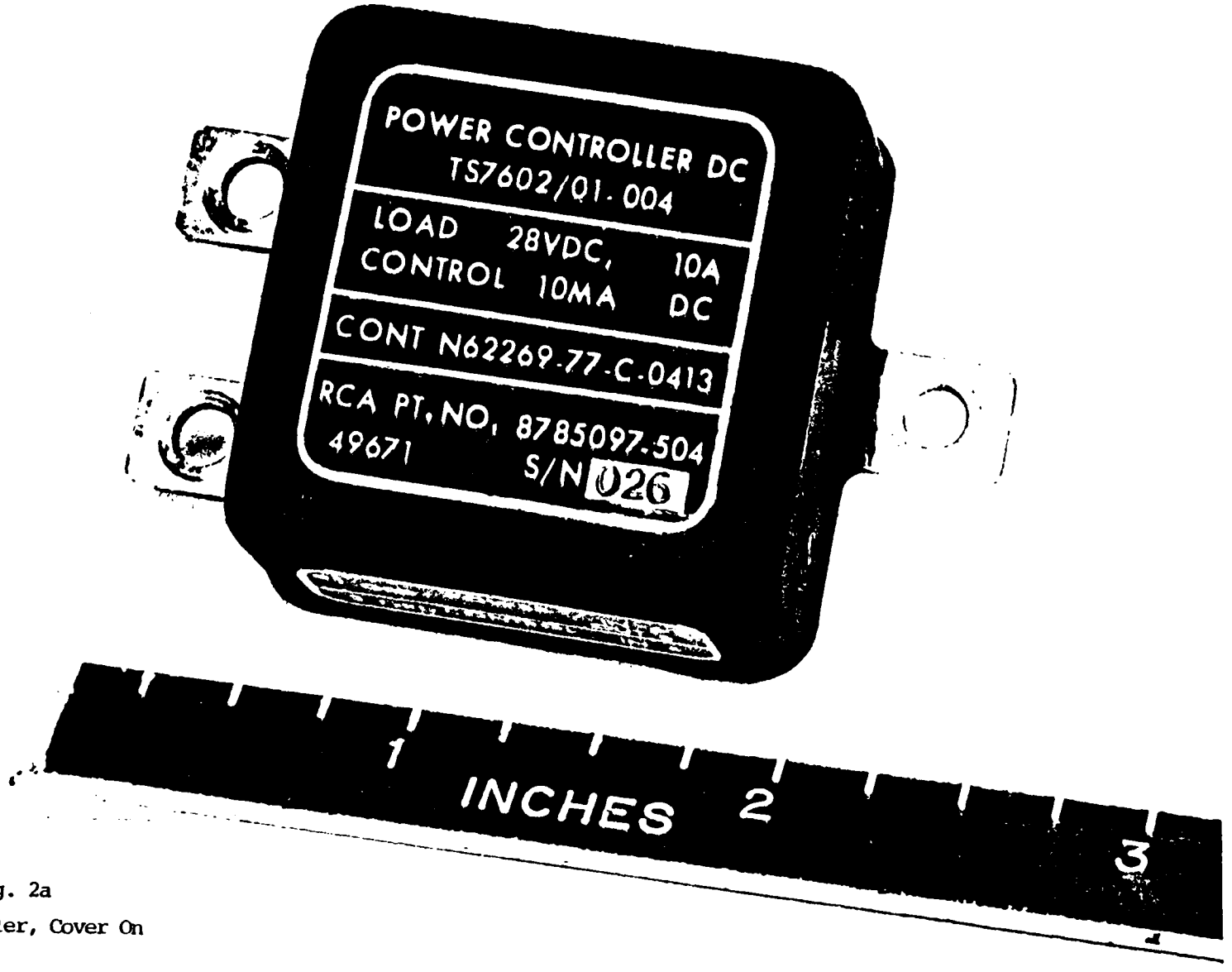


Fig. 2a
DC Controller, Cover On

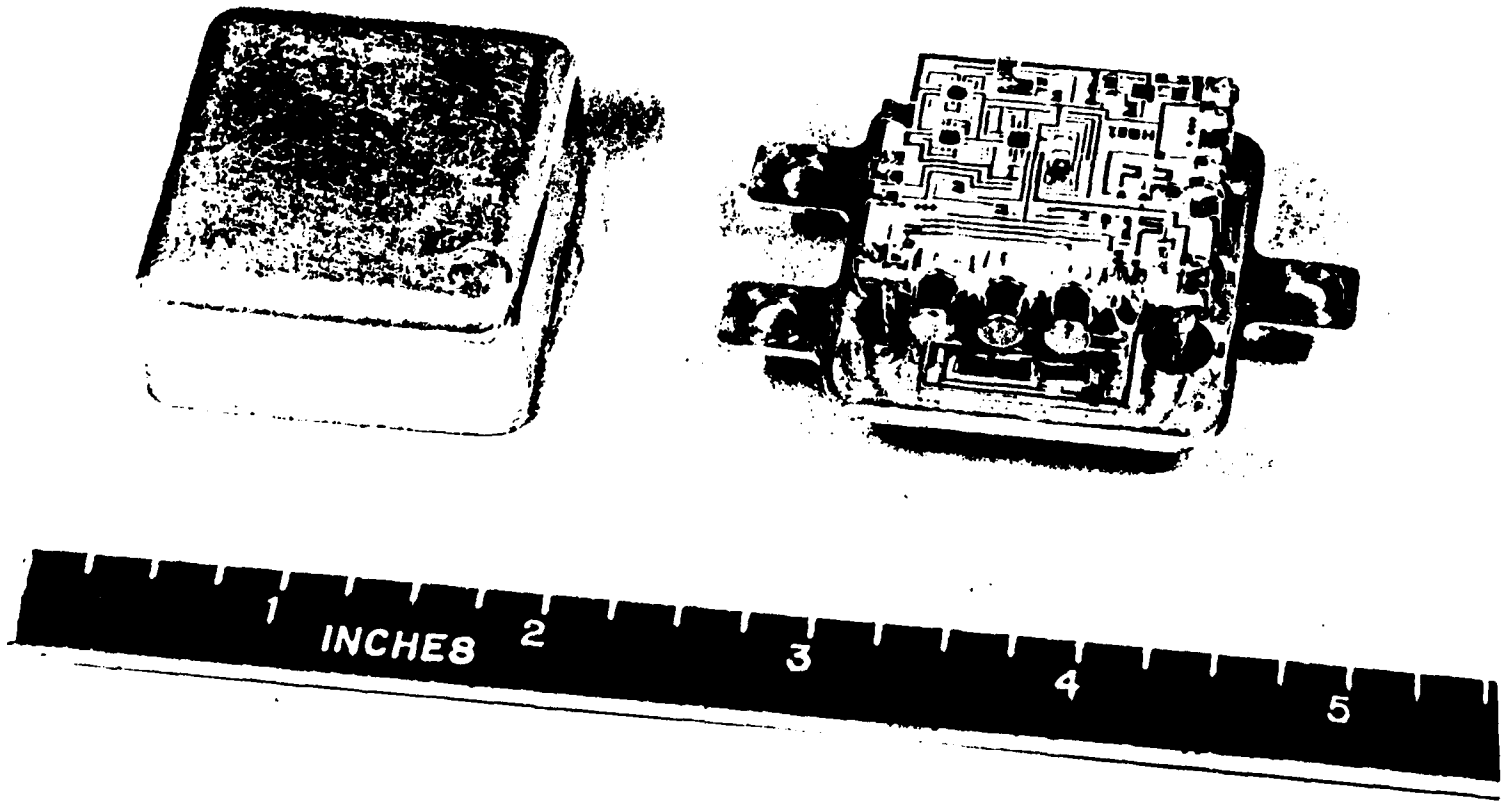


Fig. 2b

DC Controller, Cover off
Top View

RCA PC-781054-C

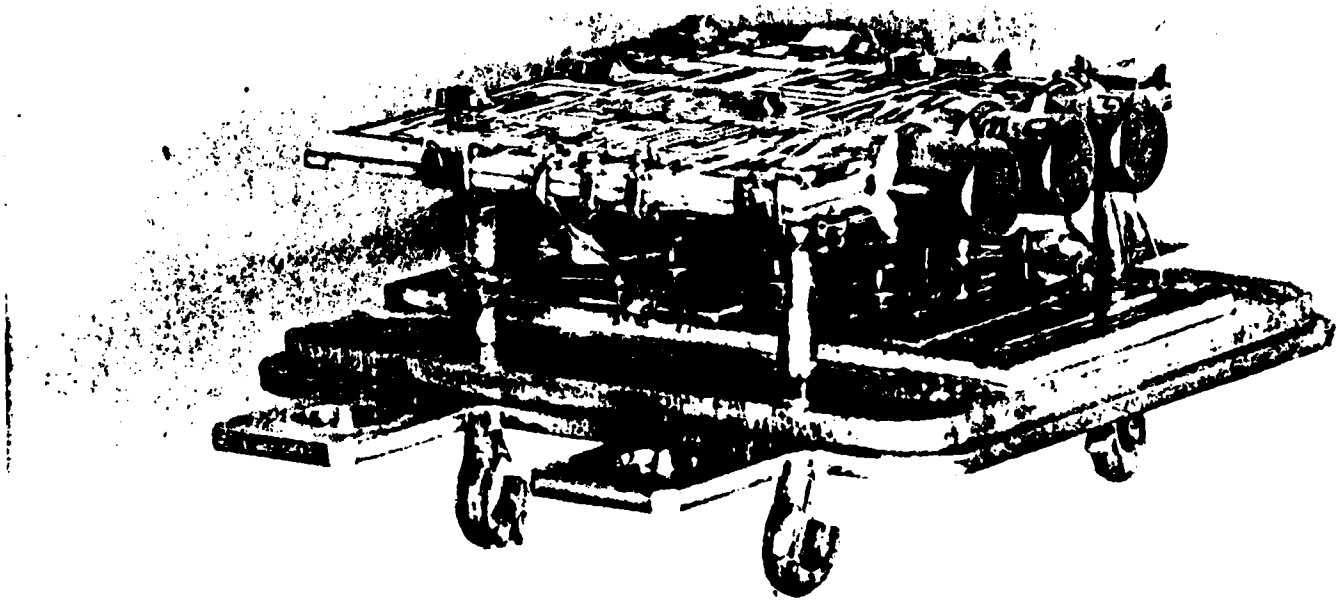


Fig. 2c

DC Controller, Cover Off
Side View

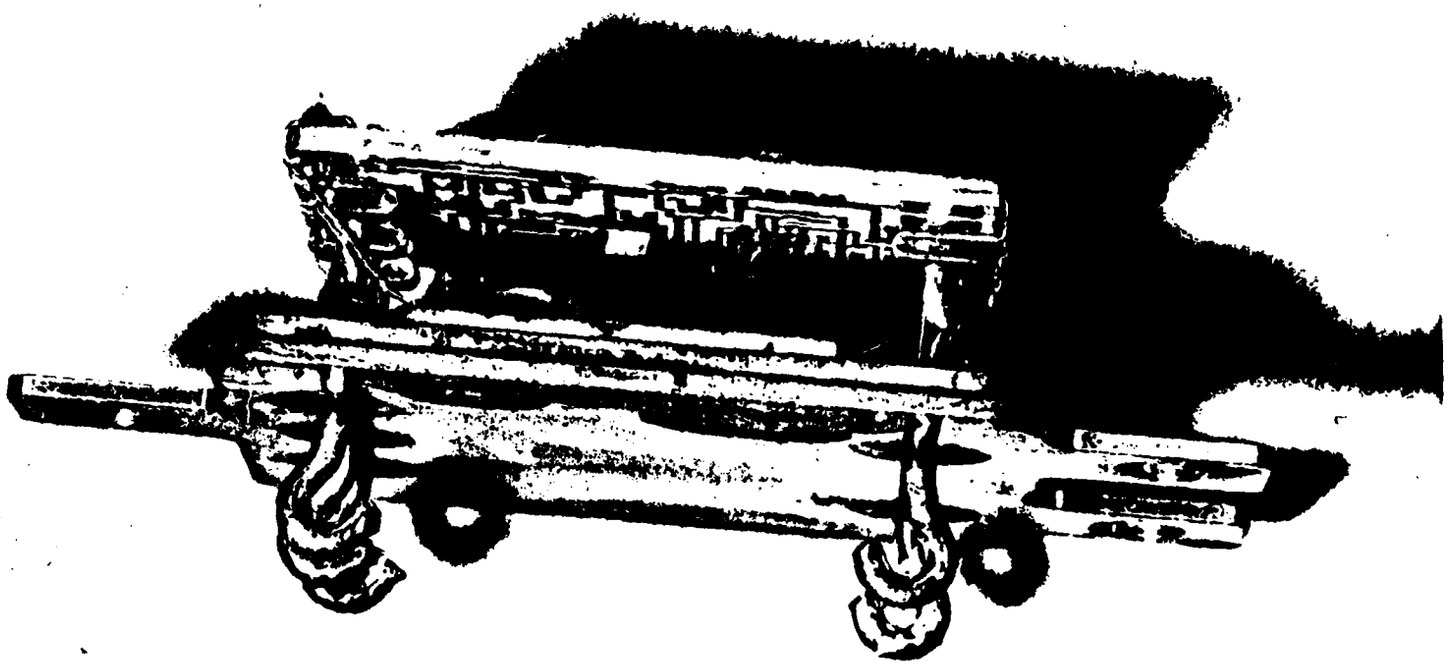


Fig. 2d

DC Controller, Cover Off
Underside View

2.2.1 Logic Subcircuit

Figure 3 shows a block diagram of the DC Controller portion contained in the outlined area at the left. The logic subcircuit consists of the control input interface, a 12.5 volt precision voltage regulator, the three CMOS IC's which perform as the internal control logic and part of the rise/fall time circuitry. Figure 4 is a schematic diagram of the logic hybrid.

2.2.1.1 Control Input/BIT Response

The control input interface circuit is composed of three optocouplers mounted off-board and discrete chip semiconductors. The circuit was designed to provide 1000 VAC RMS isolation between the controller's external control lines and the power and ground. In addition to providing a turn on signal to the control logic, the input circuit will alter its impedance between the two input terminals to indicate one of three values dependent on the operational state of the controller: 420Ω for a trip condition, 720Ω during normal operation, and 1100Ω if a fault has been detected when the input signal status is compared to the controller's output current. The input signal current is divided between the Z3 LED, used to indicate a turn-on signal to the logic, the ballasting resistor for zener diode D1, and two current sources that are set by the state of the controller. The zener diode develops a reference voltage of approximately 3 volts that is used for the Q20 constant current source. This insures sufficient LED current for proper operation of Z3 independent of the rest of the input circuitry and over the 120°C temperature range. Q1 and Q2 also act as current sources that tap a portion of the 10ma input current when they are turned on by Z1 or Z2, thus altering the circuit's effective input impedance. If the controller is in the tripped condition, both Z1 and Z2 are

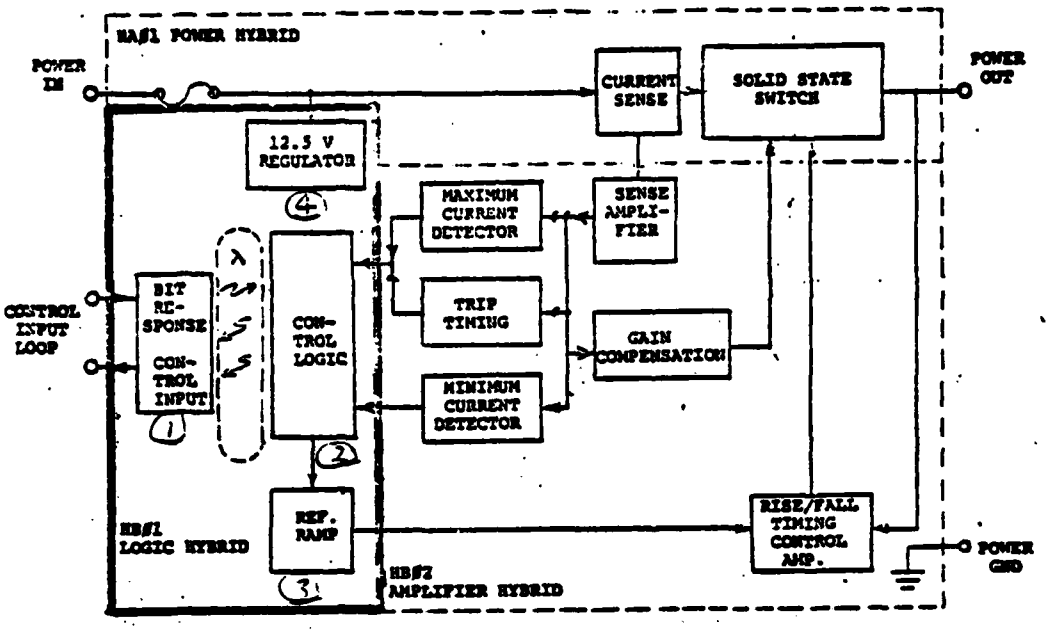


Fig. 3

Block Diagram
Logic Hybrid Outlined

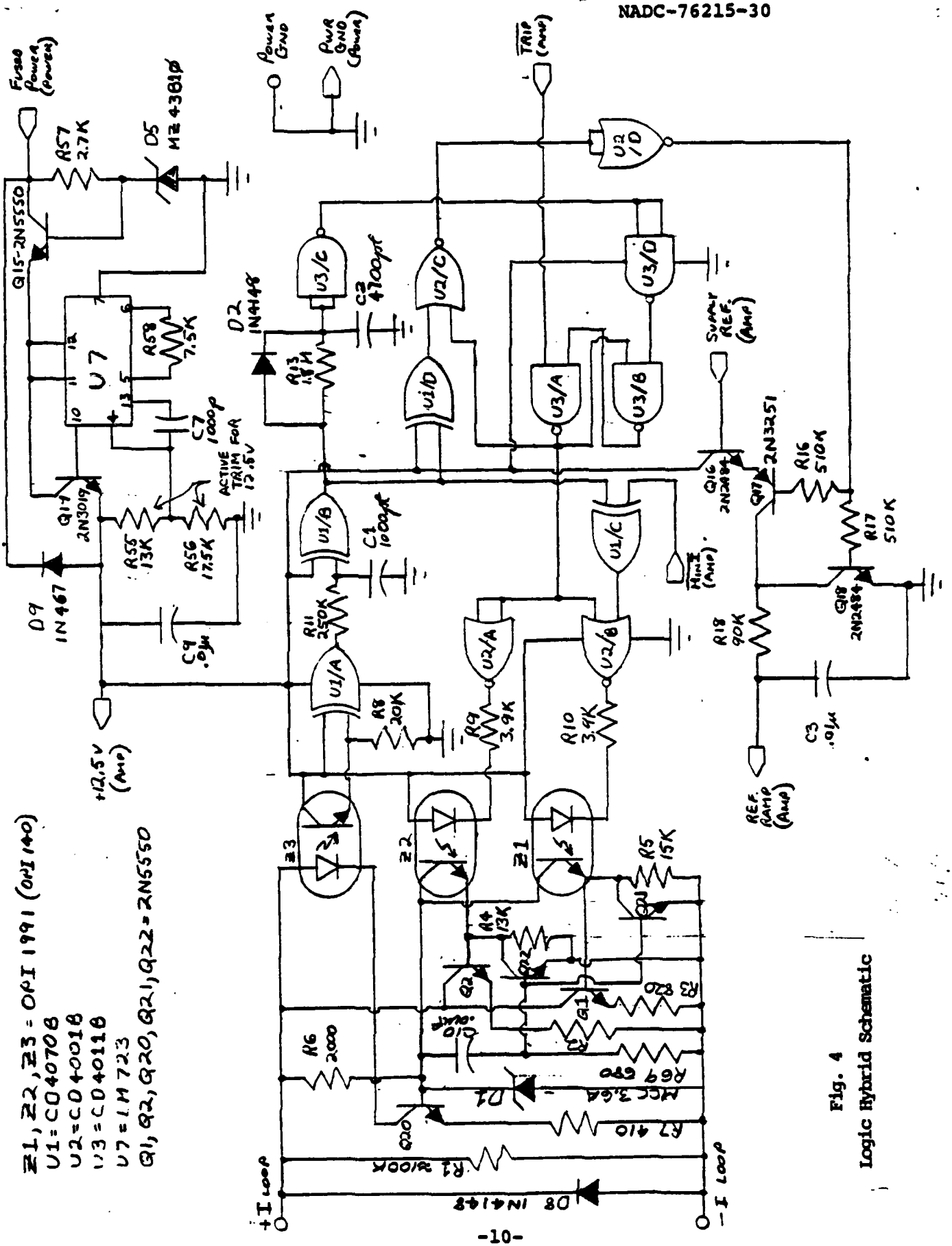


Fig. 4
Logic Hybrid Schematic

turned on with saturated photo transistors. The potential across R2 and R3 is then about .8V below the D1 zener voltage. These two paths tap a portion of the 10ma control current thus reducing the current through R6 and therefore reducing the voltage across this resistor. Under these conditions, the voltage drop across the input terminals will be about 4.2V when a 10ma input signal is applied to the controller. If the controller is in a normal operating condition, either passing output current with an applied input signal or turned off when no signal is applied, Z1 will be turned on and Z2 will be turned off. During the normal on condition, the 10ma DC input will develop 7.2V between the input terminals. During the normal off state, the controller will respond with the 7.2V level in less than 50 μs. Since the controller output will not respond in less than 100 μs, the proper off state operation of the controller may be ascertained by short duration interrogation pulses. If a fault condition is detected by the control circuitry (output current without an applied input signal or no output with input applied), both Z1 and Z2 will remain off, the input current will be divided between R6 and Z3, and the input voltage drop will be 11V. If the voltage supply is removed from the Power In terminal, there will be no supply to the logic circuitry or Z1 and Z2. Therefore, if Control Input current is applied, a fault condition will also be indicated. If the controller is delivering load current without an applied input signal, the fault condition can be sensed by application of an interrogation pulse.

2.2.1.2 Control Logic

Upon application of input signal, the transistor of opto-coupler Z1 turns on, allowing the input of buffer U1/A to go high. R11, C1, and the inverter/buffer, U1/B, will cause a 200 microsecond delay of the input signal. This will allow sampling of the BIT state of the input circuit before turning on the controller.

The output of U1/B is fed into the off-time integrator composed of R13, C2 and D2. The output of the integrator is buffered by U3/C and U3/D and fed into the reset input of the trip state flip-flop. The off-time integrator will not allow the flip-flop to reset when a trip condition has occurred until after the control input has been removed for at least 6ms.

The trip state flip-flop is composed of the two NAND gates of U3/A and B. Gate U2/C compares the output of the trip state flip-flop versus the delayed input state in order to turn on the output stage of the controller. The output of the trip state flip-flop is also buffered by U2/A and fed to opto-coupler Z2 in order to relay the trip state to the input circuit. U1/3 generates the fault status of the controller so that a fault signal will occur if either there is an input signal without detection of 10% rated controller output from Min I or if there is current output without application of input signal. The output is fed to U2/B which is lit during a no-fault state. In the event that input power to the controller is removed, the LED of Z3 will extinguish, thus also indicating the fault state.

2.2.1.3 Ref. Ramp

The output of U2/C is inverted and buffered by U2/D which feeds the bases of the PNP and NPN transistors. During an ON command to the controller, the output of U2/D is low, turning on Q17 and turning off Q18. The collector of Q17 reflects a scaled down voltage of the applied power input from the supply reference voltage developed on the amplifier hybrid. This generates an ON reference curve through R18 and C3 up to the value of the input reference voltage. This reference ramp is fed into the POWER ON amplifier on the amplifier hybrid in order to control the time of the rising and falling edge of the power output.

2.2.1.4 Regulated Power Supply

The voltage regulator IC U7 provides a stable internal supply and reference voltage over variations in temperature and power input voltage. Q15 and Zener D5, provide protection to the regulator IC input during 80 volt transients applied to the input. The 12.5 volt output taken from the buffering output of Q19 is used to supply the CMOS logic, the quad voltage comparator, quad op-amp IC's of the current detectors, and logic side of the opto-couplers.

2.2.2 Amplifier Subcircuit

Figure 5 has an outline around the Amplifier portion of the block diagram. Figure 6 is a detailed schematic of the Amplifier hybrid. The Amplifier circuitry is constructed with a quad voltage comparator U6 and a quad operational amplifier U5. These analog components provide the level sensing to detect fault and trip condi-

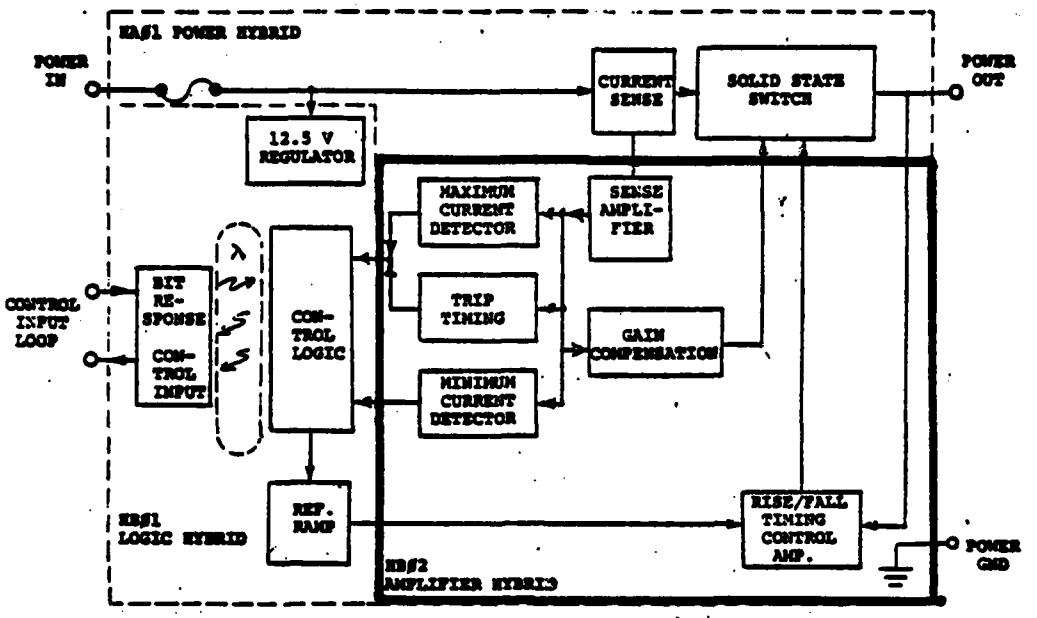


Fig. 5

Block Diagram-Amplifier Hybrid Outlined

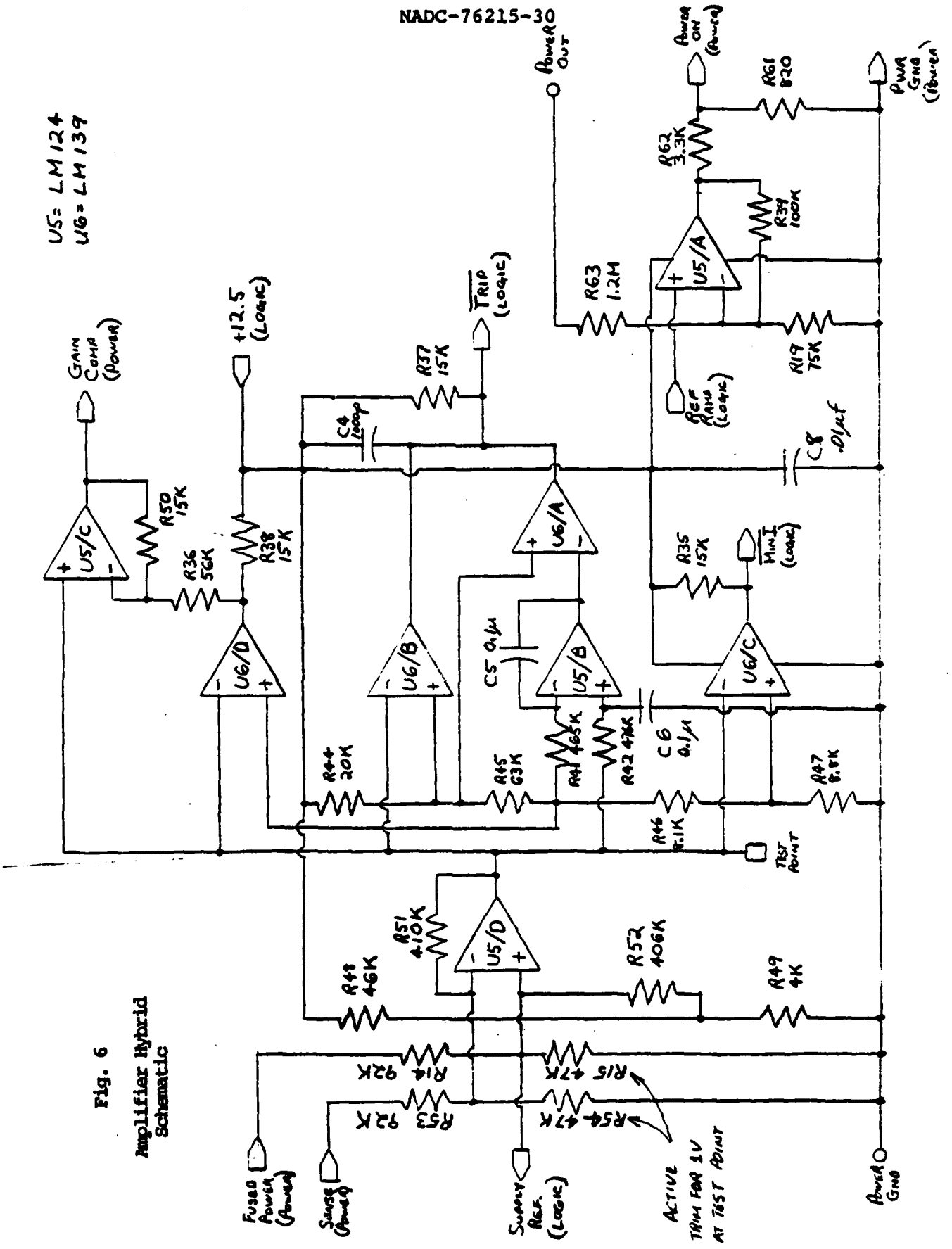


Fig. 6
Amplifier Hybrid Schematic

tions within the controller and supply the control interface to the power subcircuit.

2.2.2.1 Sense Amplifier

The current output of the controller is sensed by a proportional voltage drop referenced to the power input terminal. The resistor bridge of R14, R15, R53 and R54 provides a scaled down level of the sensed voltage to the input of the sense amplifier so that, at the maximum power input voltage of 30V, the common mode level to the op-amp is within the proper operating range. R48 and R49 provide an offset to the sense amplifier so that when the sense voltage is zero, the output of the sense amplifier will be 1V. This offset insures proper operation of the minimum current detector by increasing the common mode detection level above 0V.

The net result of the sense amplifier circuit is that for each 100% increase in the power output current to the load, the sense amplifier output will proportionally increase by .9V. Thus, with no power output current, the sense amp output will be just the 1 volt offset. At the 10% level of rated controller output, the amp output will be 1.09V; at the rated controller output current, the amp output will be 1.9V, and at 1000% of rated controller output, the sense amp output will be 10V.

The amplified sense voltage is fed into a minimum current detector of U6/C, a trip time integrator composed of U5/B and U6/A, a maximum trip limit detector of U6/B and a gain compensation amplifier composed of U5/C. The reference inputs to these four stages are derived from a voltage divider which is tied to the regulated supply of the controller.

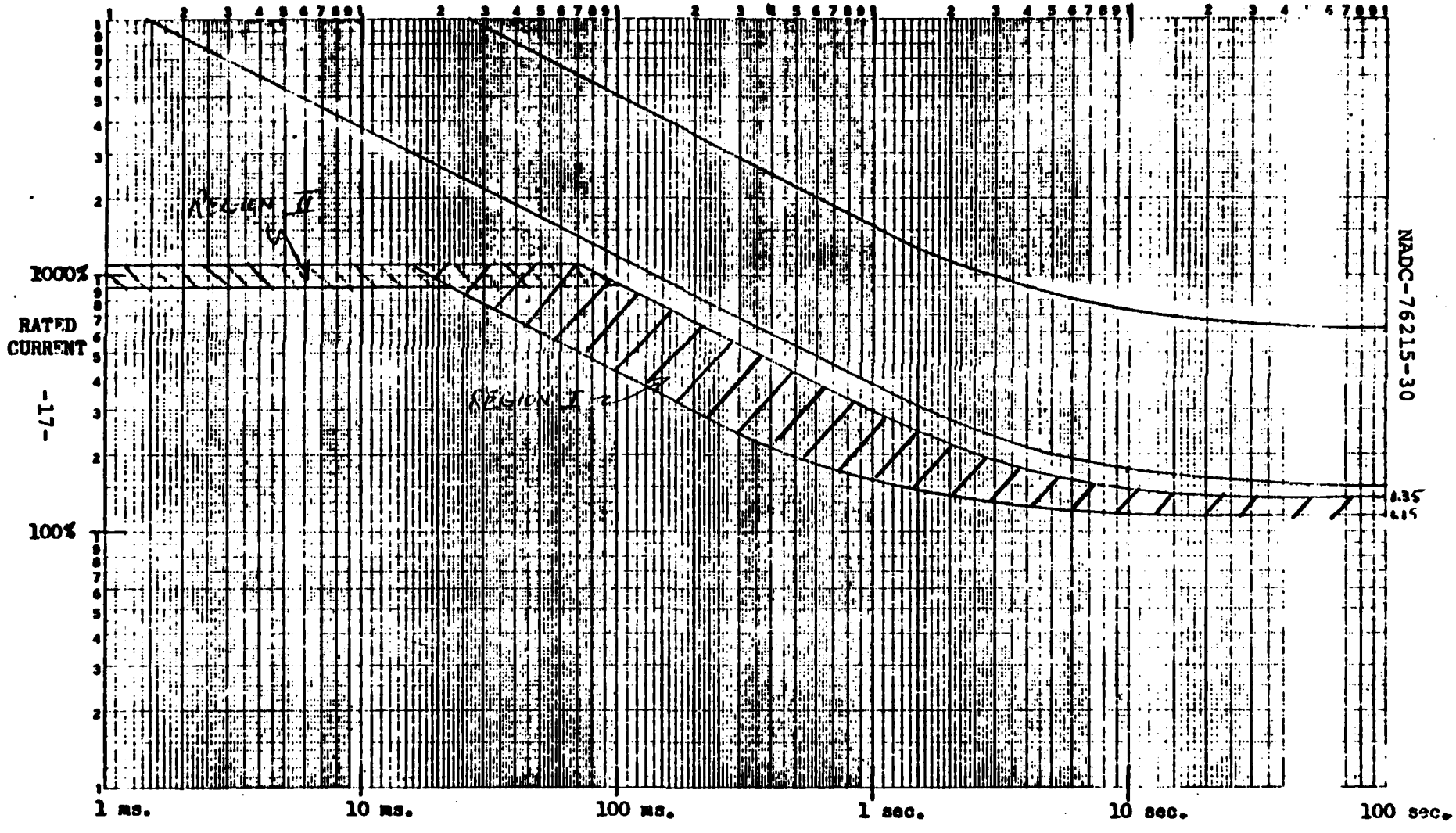


Fig. 7
Trip Timing

2.2.2.2 Minimum Current Detector

The voltage comparator, U6/B, is used as the minimum current detector and switches at the amplified sense voltage equivalent to an output of 11% rated load current. R35 is a pull up resistor tied to the comparator's open collector output so that 0 to 12.5V logic levels will be relayed to the logic hybrid.

2.2.2.3 Trip Timing

The trip time integrator, U5/B, generates a ramp voltage whose slope is in proportion to the difference of the output of the sense amplifier and the 125% rated load reference point taken between R45 and R46. Thus, the delay between application of an overcurrent condition and the time the voltage comparator, U6/A, trips low, will be in proportion to the amount of power output current that exceeds 125% of rated load. The result is a switching time in accordance with the trip timing curve as shown in Figure 7, Region I.

2.2.2.4 Maximum Current Detector

The Maximum Current Detector, U6/D, is a voltage comparator that will trip out the controller in less than 1ms when the load current exceeds 1000% of the rated output. At the 1000% level, as shown in Figure 7, Region II, the controller must trip out in less than 100ms. Since the voltage comparators of the trip time integrator and maximum current detector have open collector outputs, they may be phantom or'ed together so that either trip limit will be indicated by the low logic level at the common node.

2.2.2.5 Gain Compensation

In order to minimize the power dissipation of the controller during normal operation, extra output stage drive to the solid state switch is added only during the over-current condition. The Gain Compensation amplifier, U5/C, provides this drive as a voltage between 2.5V and 10V that is proportional to the output over-current. The voltage comparator, U6/D, inhibits the gain comp. output if the load current is less than 125% rated controller current.

2.2.2.6 Rise/Fall Timing Amplifier

The operational amplifier, U5/A, is part of a feedback loop that controls the rise and fall time of the controller's power output voltage so that proper operation can be maintained over variations in operating voltage, temperature, and nominal load current. The amplifier monitors the scaled-down voltage of the output terminal through R63 and R19, and adjusts the drive to the power switch so that the rise or falling edges of power output voltage will track a sampled section of the reference ramp generated by the control logic.

2.2.3 Power Subcircuit

The Power Subcircuit, shown in the outlined portion of the Block Diagram, Figure 8, contains the function that senses the output current to the load and provides the solid state switching of the load current. Also included on this hybrid are the components needed to suppress high voltage, short duration transients. Figure 9a is the schematic diagram of the Power

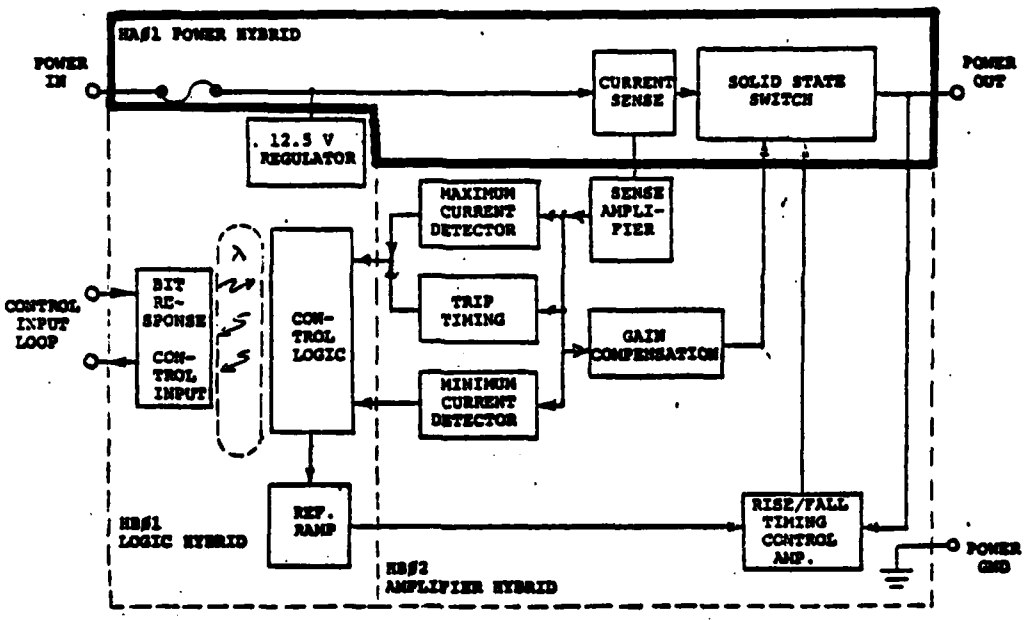


Fig. 8

Block Diagram-Power Hybrid Outlined

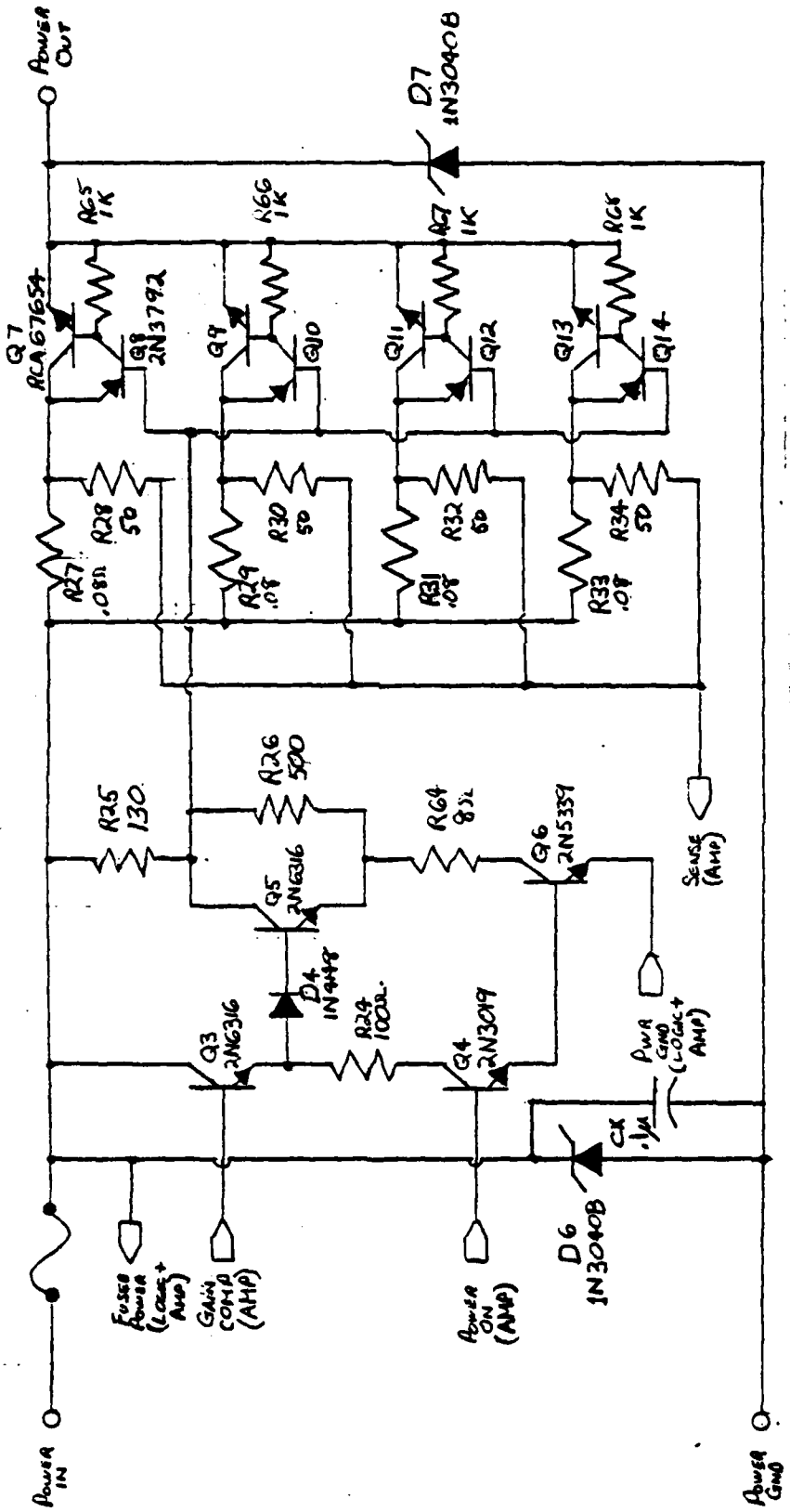


Fig. 9a

Power Hybrid Schematic-10 Amp

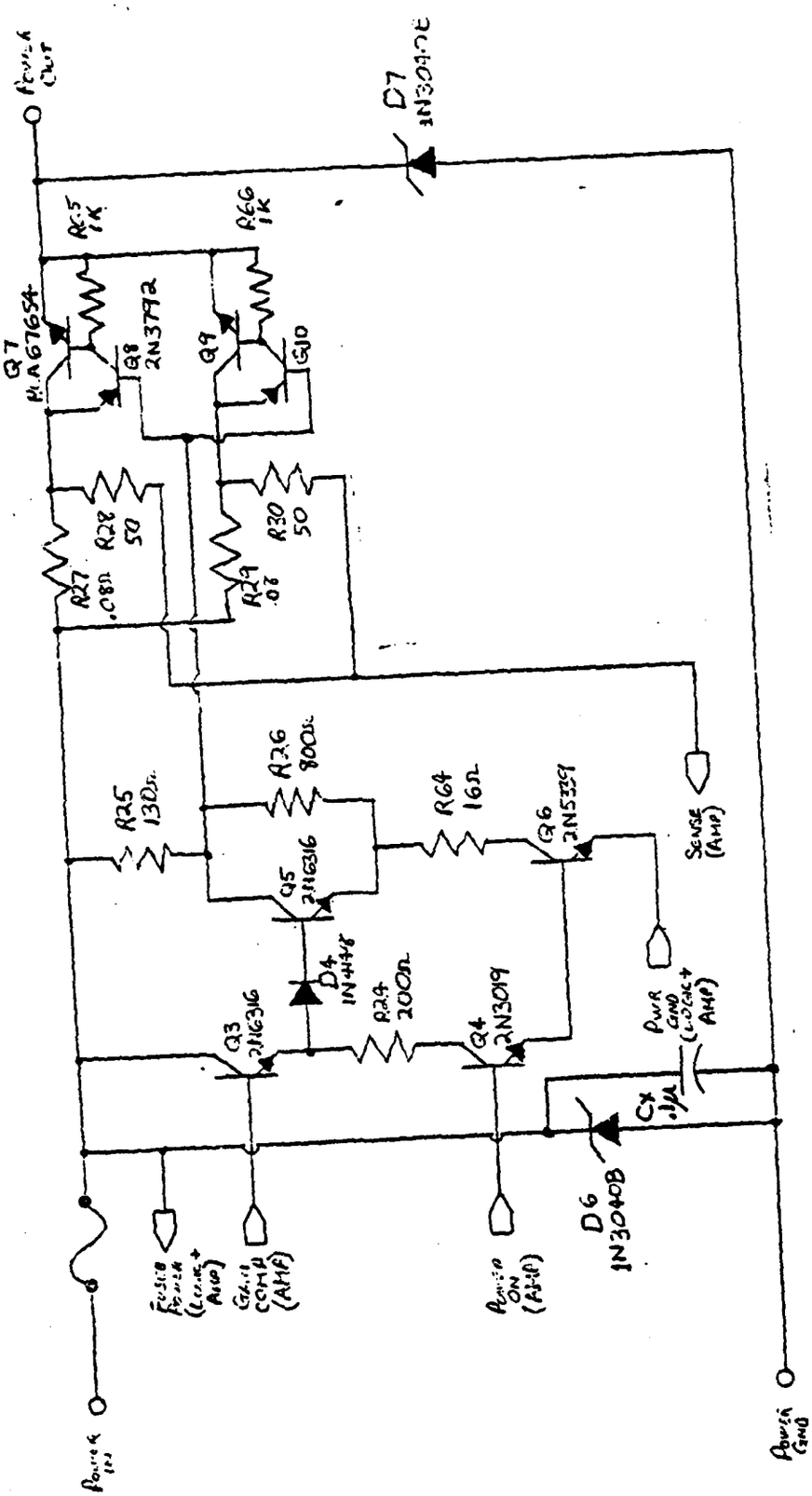


Fig. 9b

Power Hybrid Schematic-5 Amp

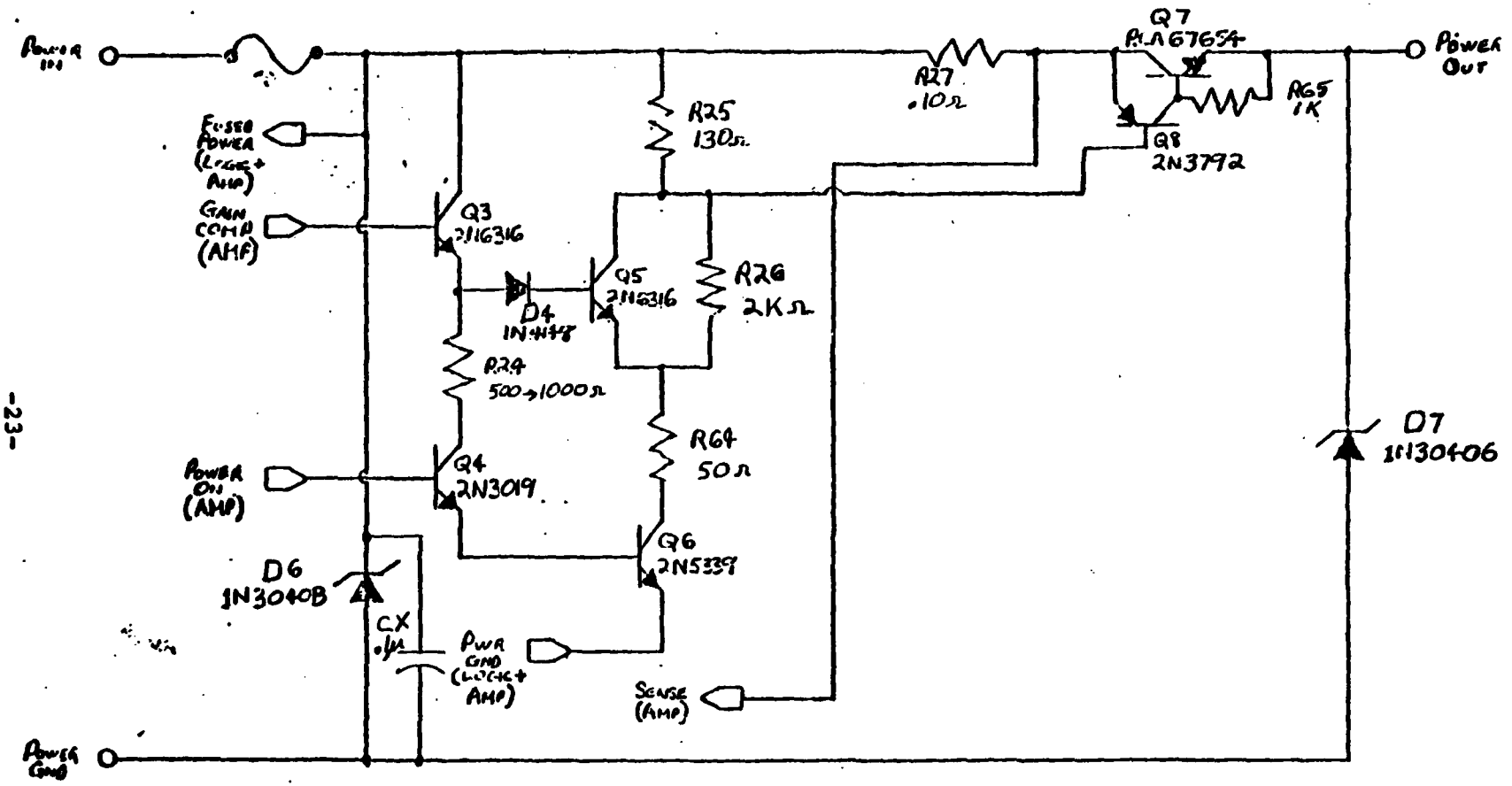


Fig. 9c

Power Hybrid Schematic-2 Amp

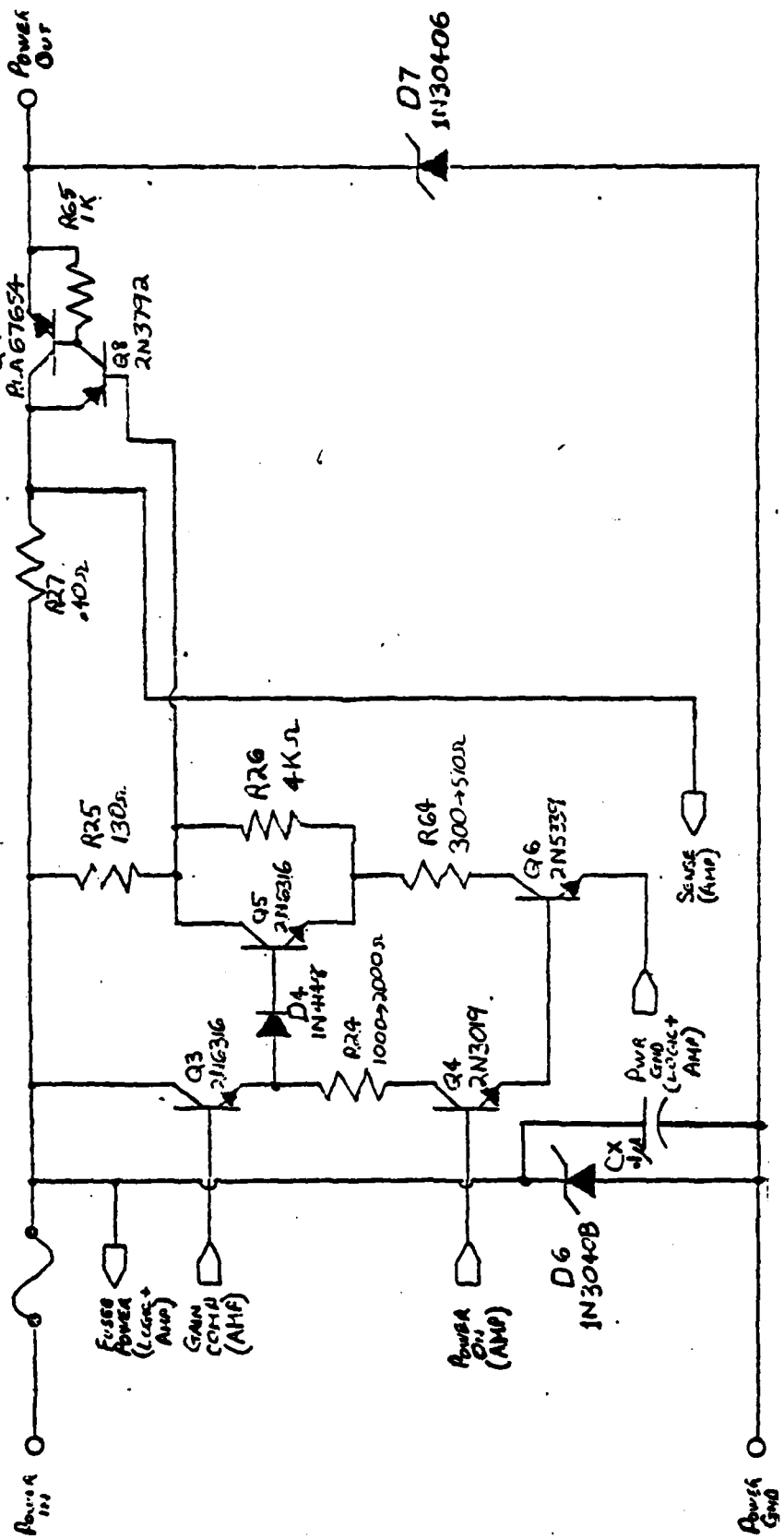


Fig. 9d

Power Hybrid Schematic-1/2 Amp

Hybrid—10 amp. version. Figures 9b through 9d are the lower current versions.

2.2.3.1 Solid State Switch

The solid state switch function can be divided into a power switching section and the control to the power switch, as shown in Figure 9. The power switch is composed of four pseudo Darlington pair stages connected in parallel for a 10A configured controller, two parallel stages for a 5A controller, and a single stage for 2A and 1/2A rated units. The output transistor of the Darlington pair was selected for its low leakage current at 100°C in conjunction with its need to deliver high currents in the on state with minimum collector to emitter voltage drop. The gain and peak current capability had to be sufficient so that at the controller header temperatures of 120°C, each Darlington pair could deliver 25 amperes. The output transistor is designed to operate just out of the saturation region in order to minimize the voltage drop from the input to output terminals and to also reduce the effects of the variation of transistor gain.

The output transistor, RCA 67654, is similar to a 2N6327 but is selected for its low leakage and guaranteed gain at low temperature. This passivated transistor also uses a fabrication technology that allows the device to be soldered to the hybrid substrate.

The drive transistor, a 2N3792, is forced to operate fully into saturation. The total voltage drop across the output pair is then the saturation voltage of the drive transistor, plus the base to emitter drop of the output transistor. The base pull down resistor of each output transistor insures minimum leakage current at elevated temperatures.

The control section of the solid state switch is similar in design over all of the controller current ratings. The semiconductor parts remain the same for all controllers but, in order to reduce the on stage power dissipation, the resistor values selected are depndent on the controller output current rating.

During normal operation up to rated output current, the GAIN COMP input insures that Q3 is turned off and that the control to the solid state switch is applied from the POWER ON lead from the amplifier hybrid. Since Q3 is off, there is no supply current to the collector of Q4, or the base of Q5, therefore eliminating them from acting as gain stages. The base drive to Q6 is therefore only the current supplied from the POWER ON input. The drive to Q6 insures that it is saturated. Since Q5 is inactive, the drive current to the power switching section is determined predominantly by R26. This resistor value is determined by the worst case gain condition of the output when the POWER IN terminal is held at 17.5V. During an overcurrent condition, the GAIN COMP signal increases in proportion to the output current, thus turning on Q3. This now allows Q4 to supply extra drive to Q6 to maintain it in saturation and also allows Q5 and R64 to act as a current source. The result

is then the added drive current required by the output transistors during the high load current surges, but without effecting the power dissipation during normal operation.

2.2.3.2 Current Sense

Detection of the controllers output current is achieved by the placement of thick film resistors in series with the output current path. Each output transistor pair has a sense resistor that is specified to have .2V drop when the stage is passing its rated capability. Since for 10A and 5A controllers the individual output stages are designed to pass 2.5A when delivering rated capacity, the sense resistor value used would be 80 milliohms. The 2A and 1/2A controllers only use one output stage and therefore the sense resistors used with those units would be 100 mΩ and 400 mΩ respectively.

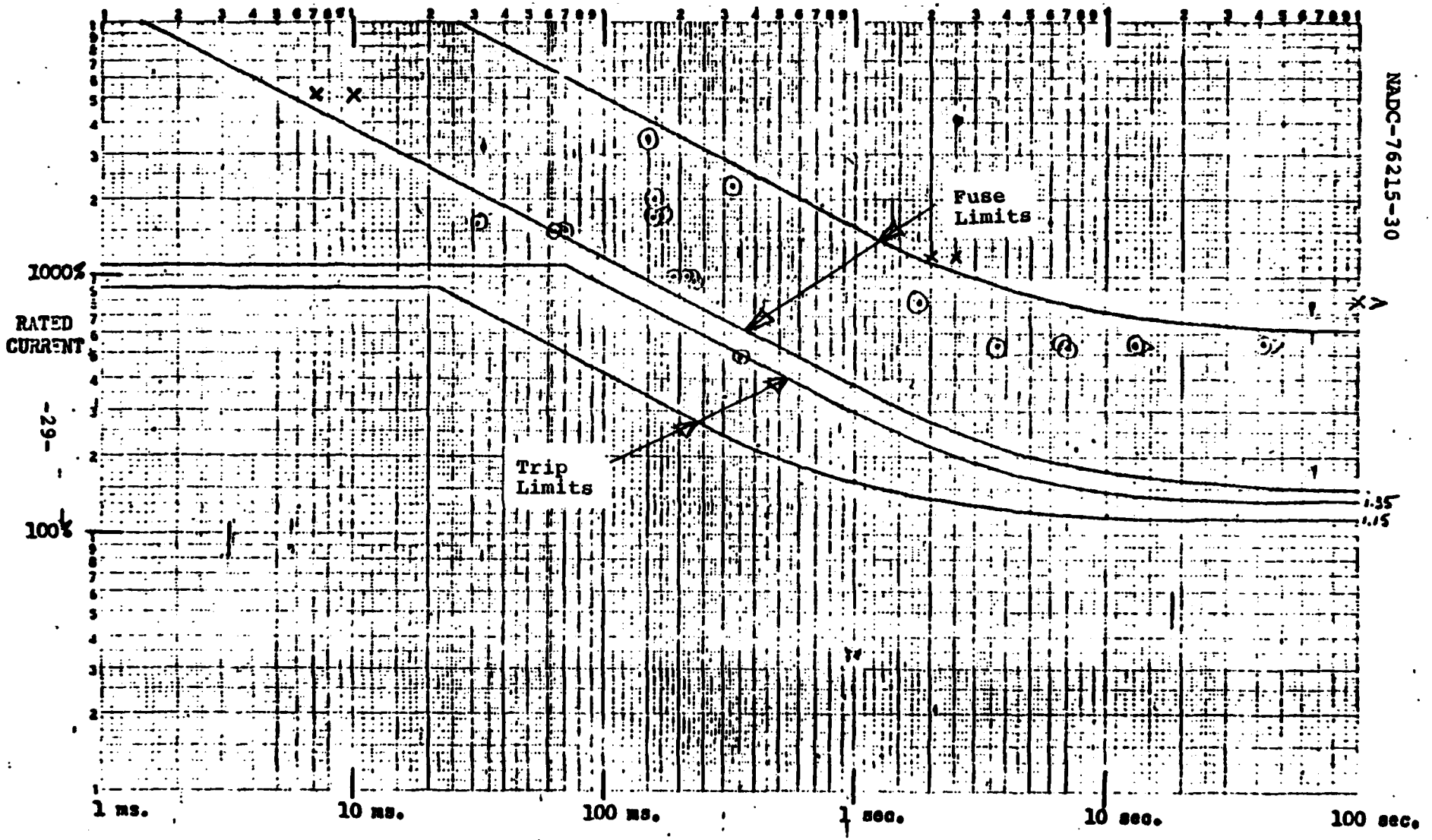
The sense resistors also provide a ballasting effect in the multiple stage 5A and 10A controllers. In the event that any single output stage begins to pass more current than any other parallel stage, the sense drop of that series resistor will increase, thus reducing the emitter to base drop of that particular drive transistor. This will reduce the drive current to the dominant output transistor.

The sense resistor voltage drops are summed together through 50Ω resistors to a common node. The summing resistors also provide isolation between stages so that the ballasting effect can be maintained.

The sense resistors also provide the fail-safe fusing function. Experiments with a separate fuse wire that would have been incorporated as part of the power hybrid, did not provide confidence for repeatable unit-to-unit results. Sense resistors subjected to over-current surges would blow out more uniformly as shown in Figure 10. The results indicated that the resistors would open above the valid fusing curve at the lower overload currents and that they would not blow out in the valid trip-out region. Results using the coil were as a fuse element indicated that violation of the power controller trip area was possible (See Figure 10).

> = Fuse would burn at greater than indicated time
⊙ = 28 G Coil wire 230 mil long loop
X = Untrimmed 80 mΩ sense resistor

10A Controller Fuses



NADC-76215-30

Fig. 10
Sense Resistor Fusing Characteristics

3.0 PHYSICAL DESIGN

The controller mechanical design required minimization of the volume and weight but with a rugged construction that could withstand 100G's of shock and a rigorous vibration cycle. In order to meet these requirements, plus a -65°C to 150°C storage temperature, the controller circuitry was contained within a steel cover mounted to a cold rolled steel header base plate. Figure 11a is a sketch of the design.

3.1 Header and Cover

The design for the controller package as dictated by Specification No. NADC-30-TX-7602/01, required five terminals to be mounted on the base plate assembly. Since open semiconductor chips were used in the design, the package was required to be hermetic. Hence, in order to make contact with the internal circuitry, the terminal posts used a glass to metal terminal to isolate them from the metal header.

Initial calculations indicated that using the .200 inch terminal spacing specified by the slash sheet would not allow the controller to pass the required dielectric withstanding voltage test at a pressure equivalent of 100,000 feet altitude. Tests were performed assuming a .350 inch terminal spacing and using a .250 inch diameter glass bead. Under a 500V potential, this design withstood voltage breakdown until the 70,000 foot equivalent pressure was reached. To incorporate the large insulation spacing required, the header layout was altered to that shown in Figures 11a, 11b and 11c, and terminal hooks were incorporated as per NADC request.

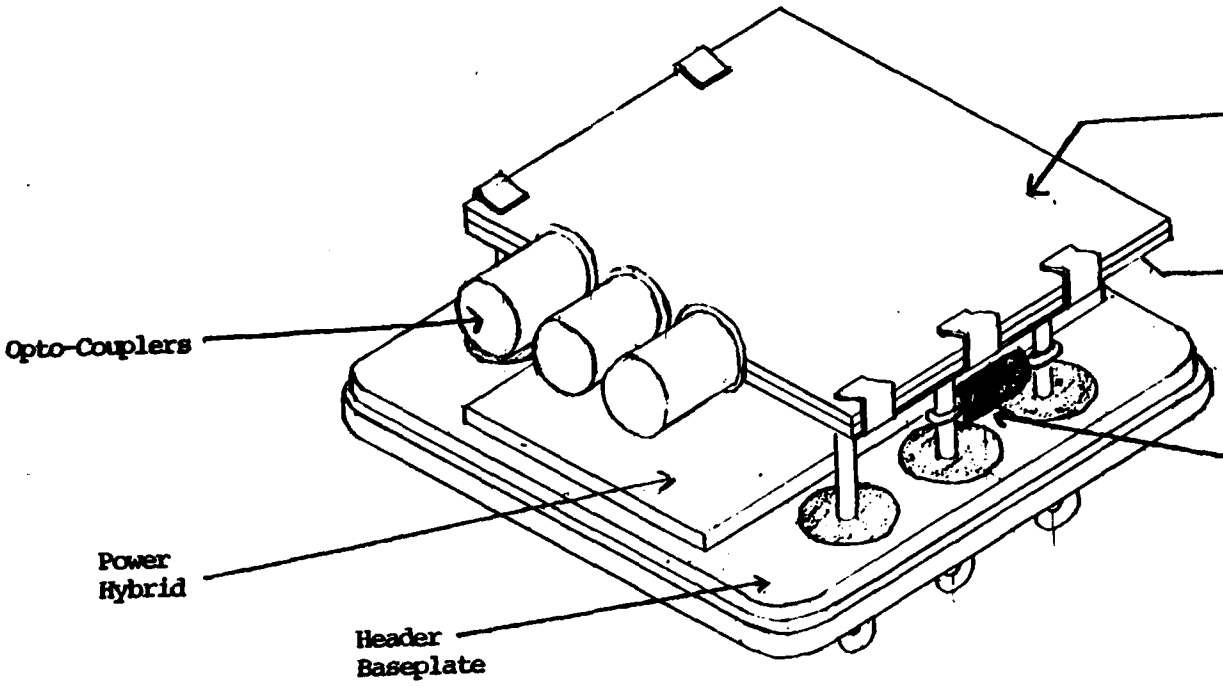


Fig. 11a

Package Design

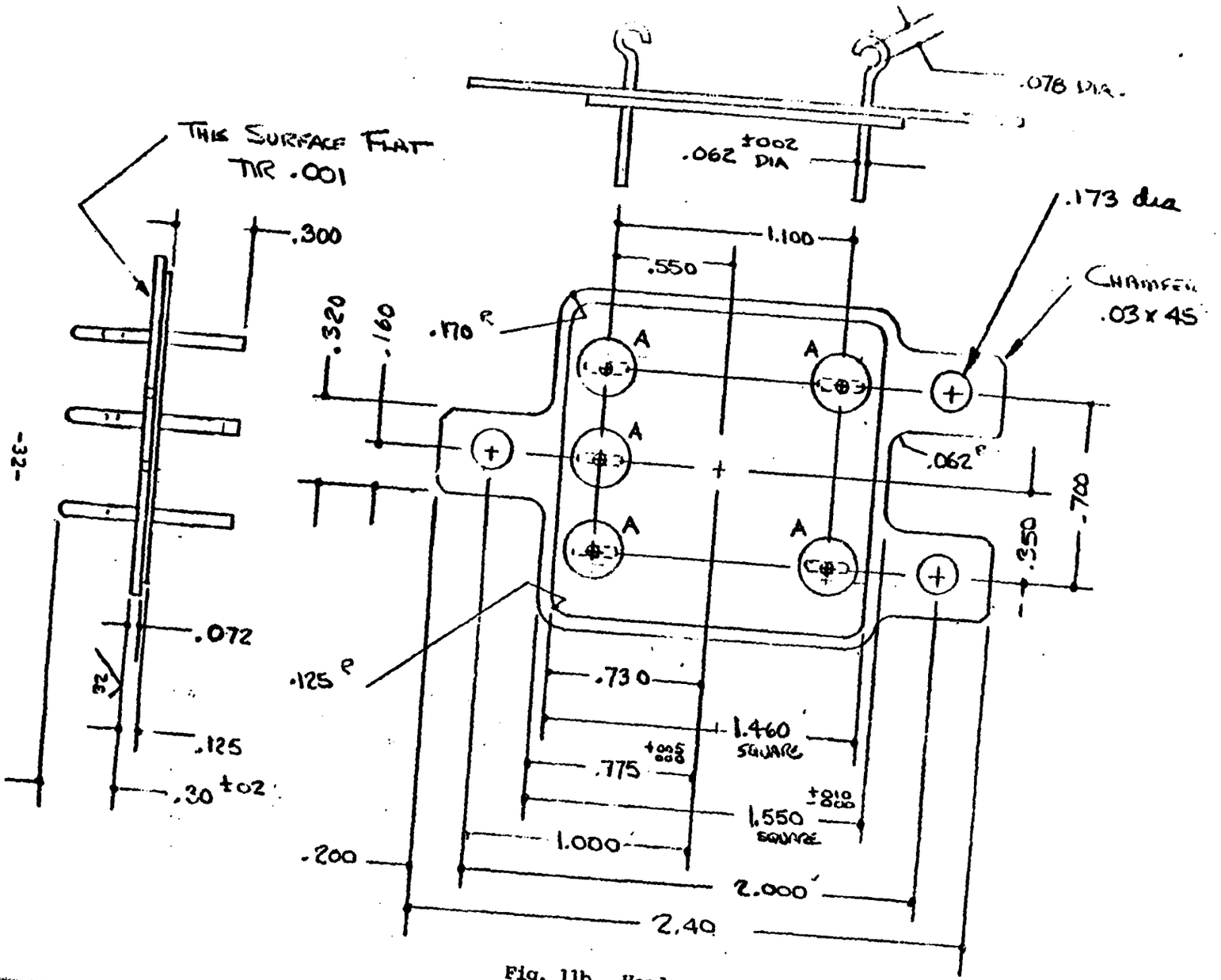
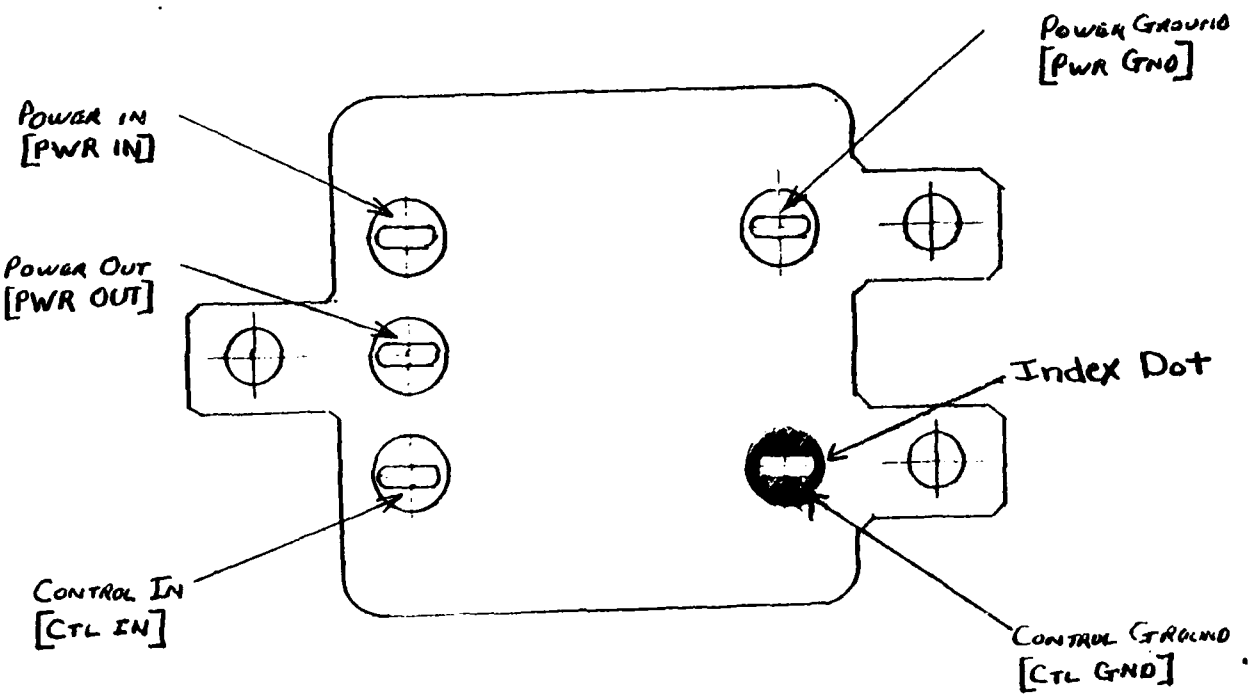


Fig. 11b Header Layout



Bottom View

Fig. 11c

Header Connections

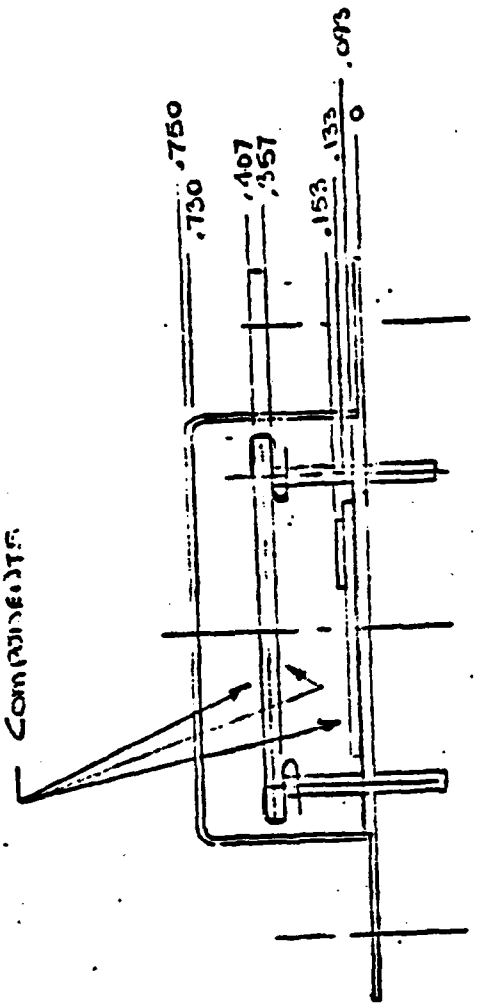


Fig. 11d
Cross Section

Due to the similar internal construction of all controllers, only one type of cover was manufactured for all controller ratings. This tin plated steel cap was then soldered to the plated header after the hybrids were installed. An evacuation hole in the top of the cover provided the final seal.

3.2 Internal Construction

As shown in Figure 11a and 11d, the three hybrids that contain all the controller circuitry are arranged in two separate layers. The bottom layer is the power subassembly and consists of the header baseplate, the power hybrid and a discrete diode. The top layer is the control subassembly and is composed of the logic and amplifier hybrids, and three opto-couplers.

3.2.1 Power Subassembly

The power subassembly identifies the controller's output current rating by the capacity of the power hybrid soldered to it. In order to minimize the thermal resistance between the power transistors and the header heat sink, beryllia oxide was selected for the power hybrid substrate. The power hybrid is fabricated from .040 inch thick beryllia, with a final thick film copper backplane and copper metallization on the top surface.

Copper metallization was specified because of its good electrical conductivity, reduced metal scavaging during the high temperature soldering of power transistors, and lower thermal resistance than other types of metallization.

Major power transistors used a soldered back technology and the lower current semiconductors were attached with conductive epoxy.

Interconnection to all but the power output transistors was made with appropriate size and number of gold wire bonds. The power transistor emitter and base contacts were made with clips attached to brass posts. As indicated in Figure 12, the posts were supported and aligned by holes placed in the beryllia. After the posts were soldered to the copper metallization, the alignment hole was then backfilled with epoxy to provide an insulating barrier.

Screened, thick-film resistor chips were used on the power substrate. Using chip resistors provided the advantage of having to manufacture only one type of (BeO) substrate, then selecting the chip components dependent on the power hybrids current rating.

A discrete 1N4002 diode was incorporated into the power subassembly by supporting it between the POWER IN and POWER OUT terminal posts. The axial leads of this device then provided the mechanical and electrical connection to the subassembly.

3.2.2 Control Subassembly

The top level of the controller circuitry is constructed of the logic and amplifier hybrids placed back-to-back and supported

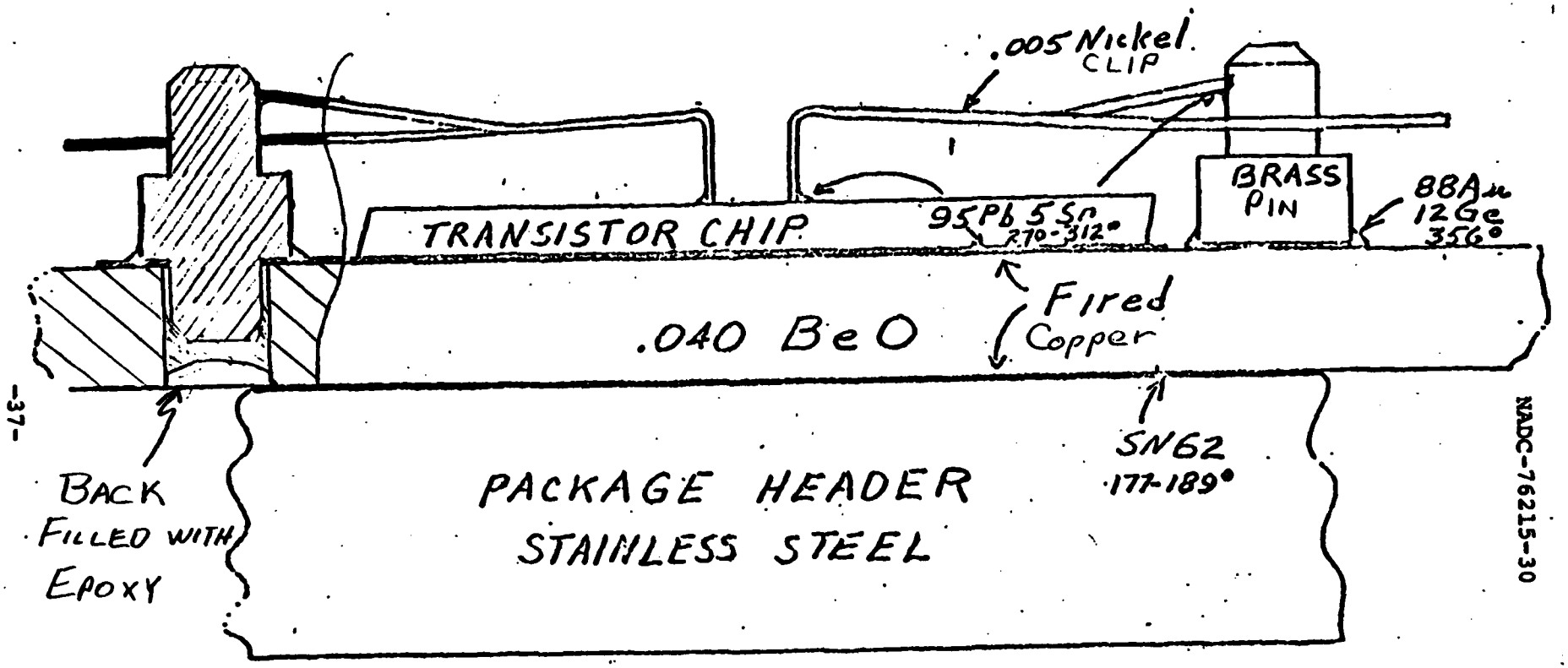


Figure 12.

Cross-Section of Power Hybrid

by five header terminal pins. Besides providing the mechanical support to hold the subassembly firmly in place, four of the five terminal pins also are used for the electrical connections to the lower level. Two of the terminal pins bring the control input signal directly from the outside, up to the logic hybrid. One other pin ties the ground to the subassembly and the final pin connection monitors the response of the power out terminal.

Five riser wires provide additional interface between the upper and lower levels. The wire contacts are made by solder connection directly to the power hybrid metallization and to the wrap-around clips on the upper level. The wrap-around clips also provide the electrical interconnection between the logic and amplifier hybrids.

Three opto-couplers are cantilevered on one side of the upper assembly. These TO-18 case units make mechanical and electrical connection via the four wire leads which protrude from the bottom of the opto-coupler as indicated in Figure 13. Electrical interconnection from the lead contacts on the amplifier hybrid side to where the input circuit resides on the logic hybrid, is made with copper straps.

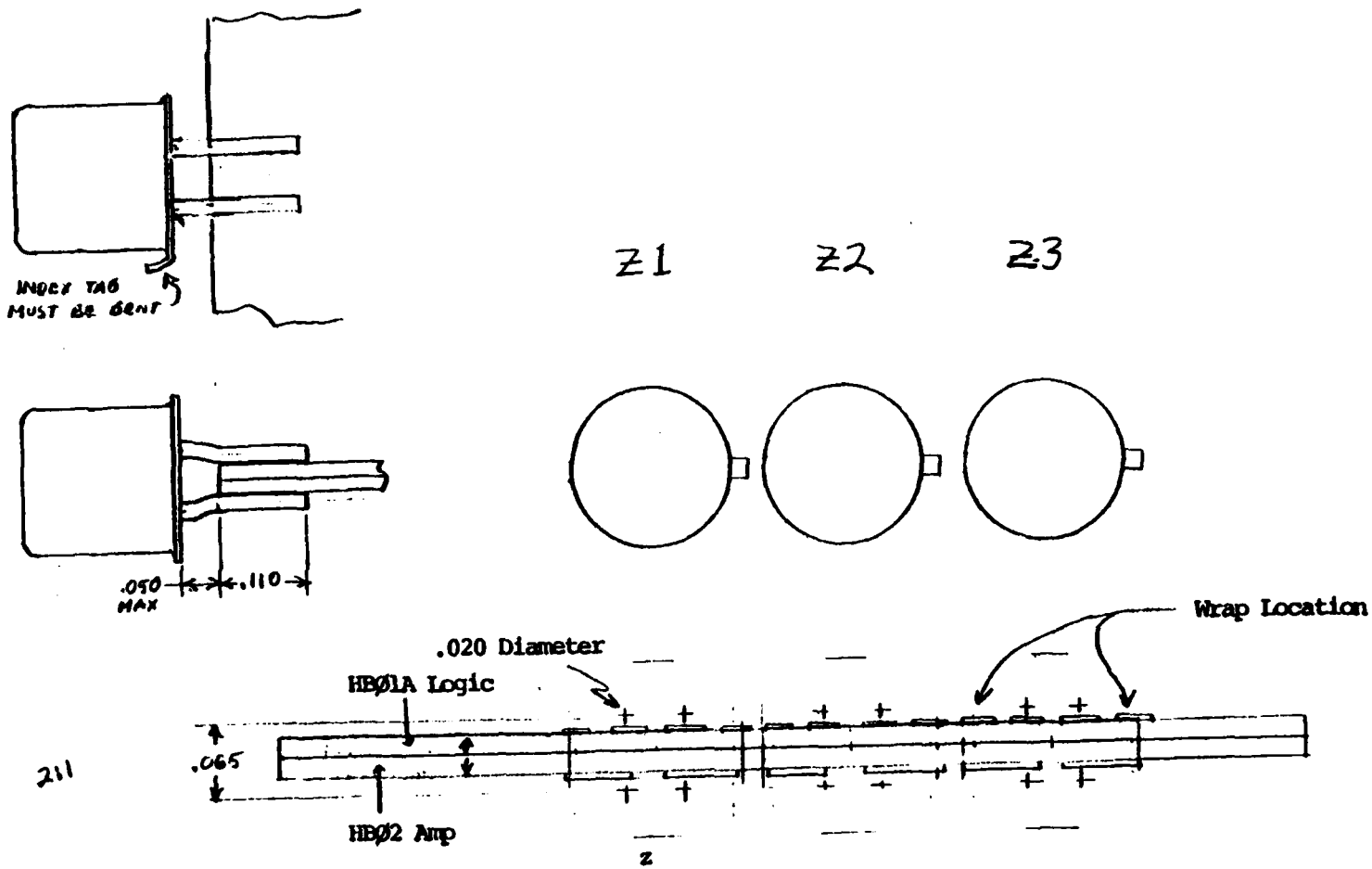


Fig. 13

Opto-Coupler Orientation

4.0 MANUFACTURING AND TESTING

The sequence for producing an integrated controller involved first, the construction of the three hybrid types, then assembling each subassembly, and then final integration and seal.

Parts were tested throughout the production cycle so that any circuit failure could be detected as early as possible and to also insure that the controller, when sealed, would fully comply with the specification requirements. Figures 14 a, b and c detail the assembly and testing steps required from substrate printing to delivery of completed and tested controllers.

4.1 Control Subassembly

Similar construction sequences were used to assemble the logic and amplifier hybrids. At steps L1 and A1, as shown on Figure 14a, the substrate was constructed with multiple levels of printing of thick film resistor and conductor traces. Trimming resistors to value was also included at this production level. At the second level (L2 and A2), semiconductor chips were epoxied to the substrate and, after a high temperature cure, these parts were wire bonded to the substrate to make their electrical connections. After bonding, the hybrids were checked for proper operation.

DC CONTROLLER PRODUCTION FLOW 29
PAGE 1
LOGIC/AMP

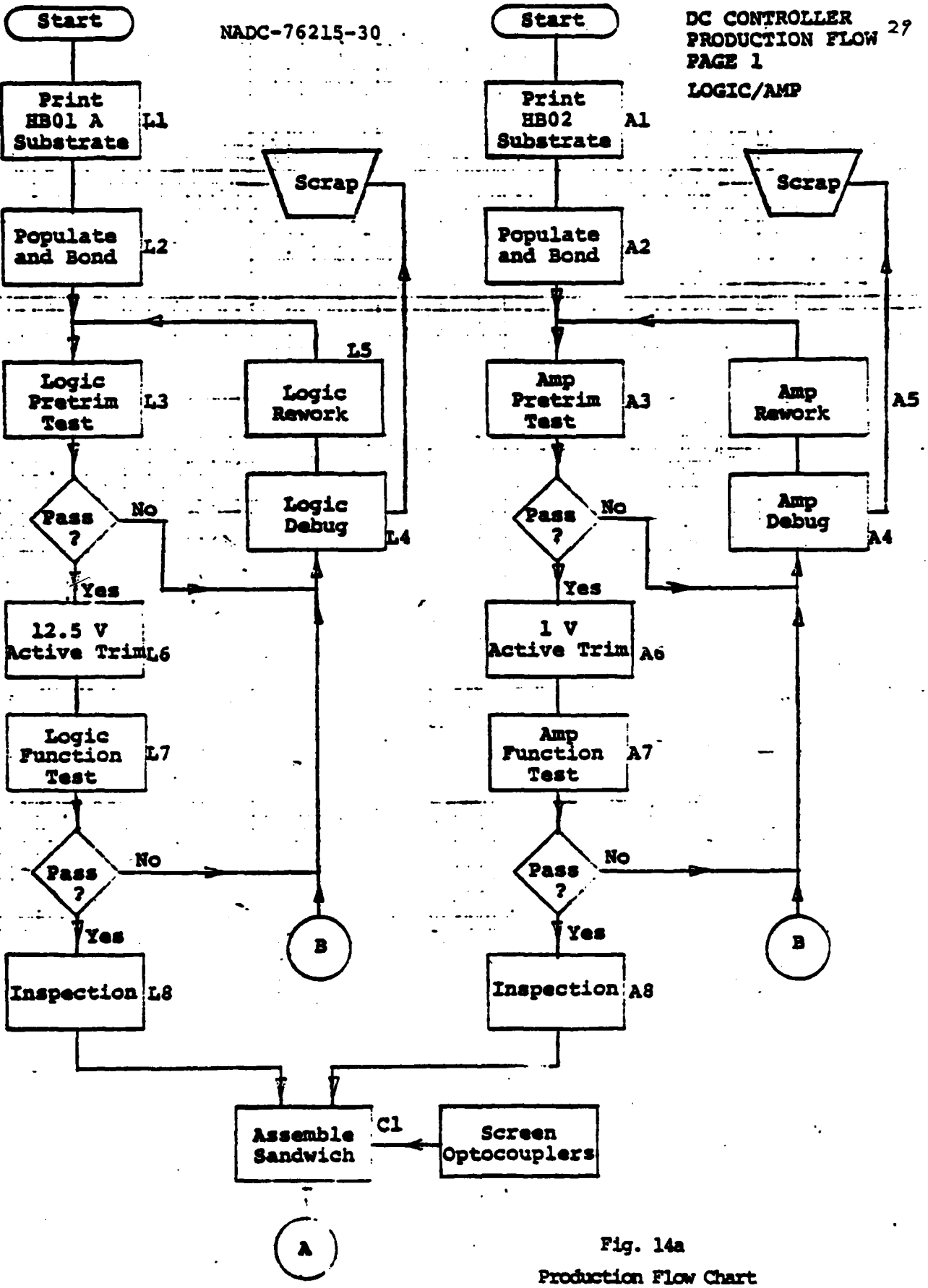


Fig. 14a
Production Flow Chart

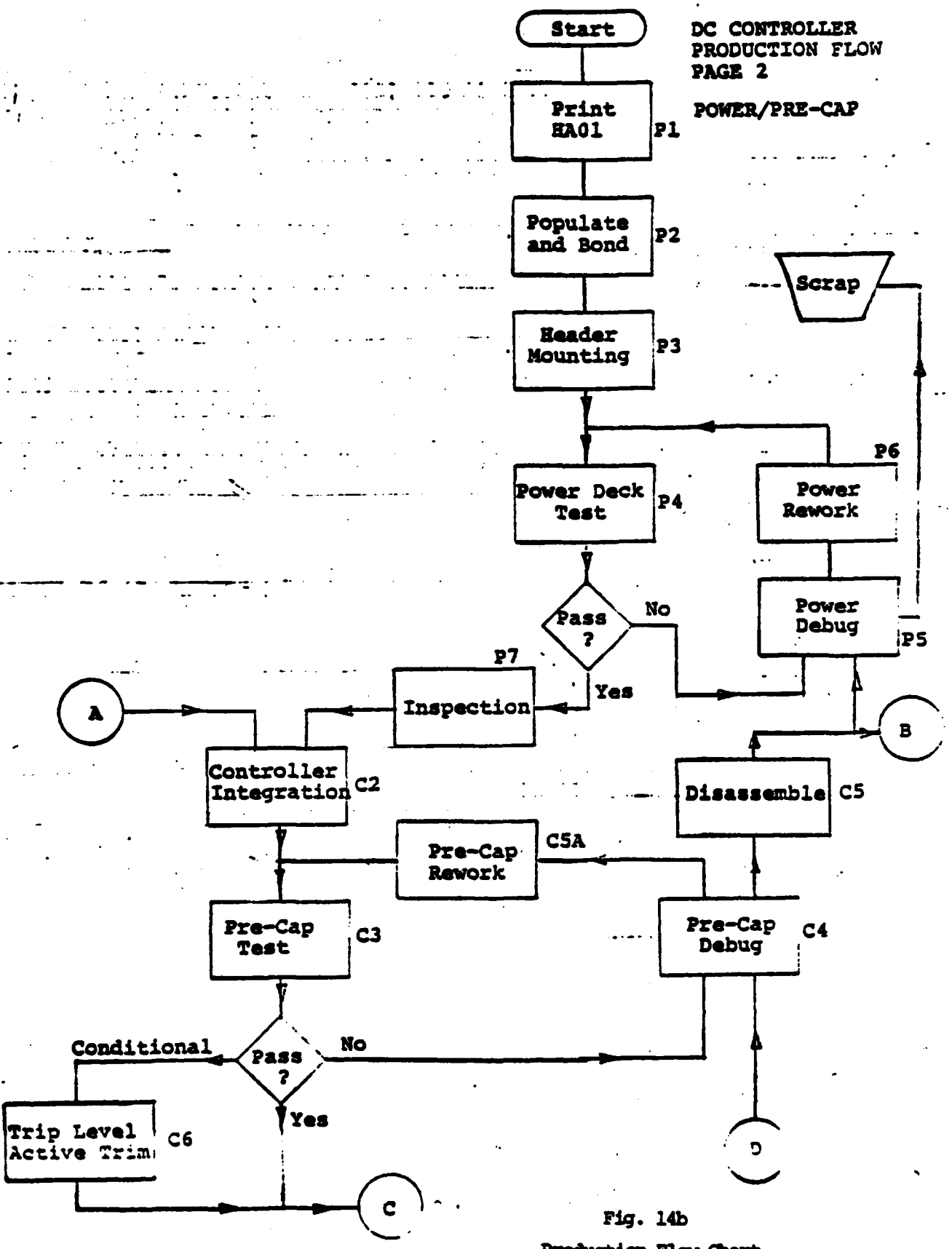


Fig. 14b
Production Flow Chart

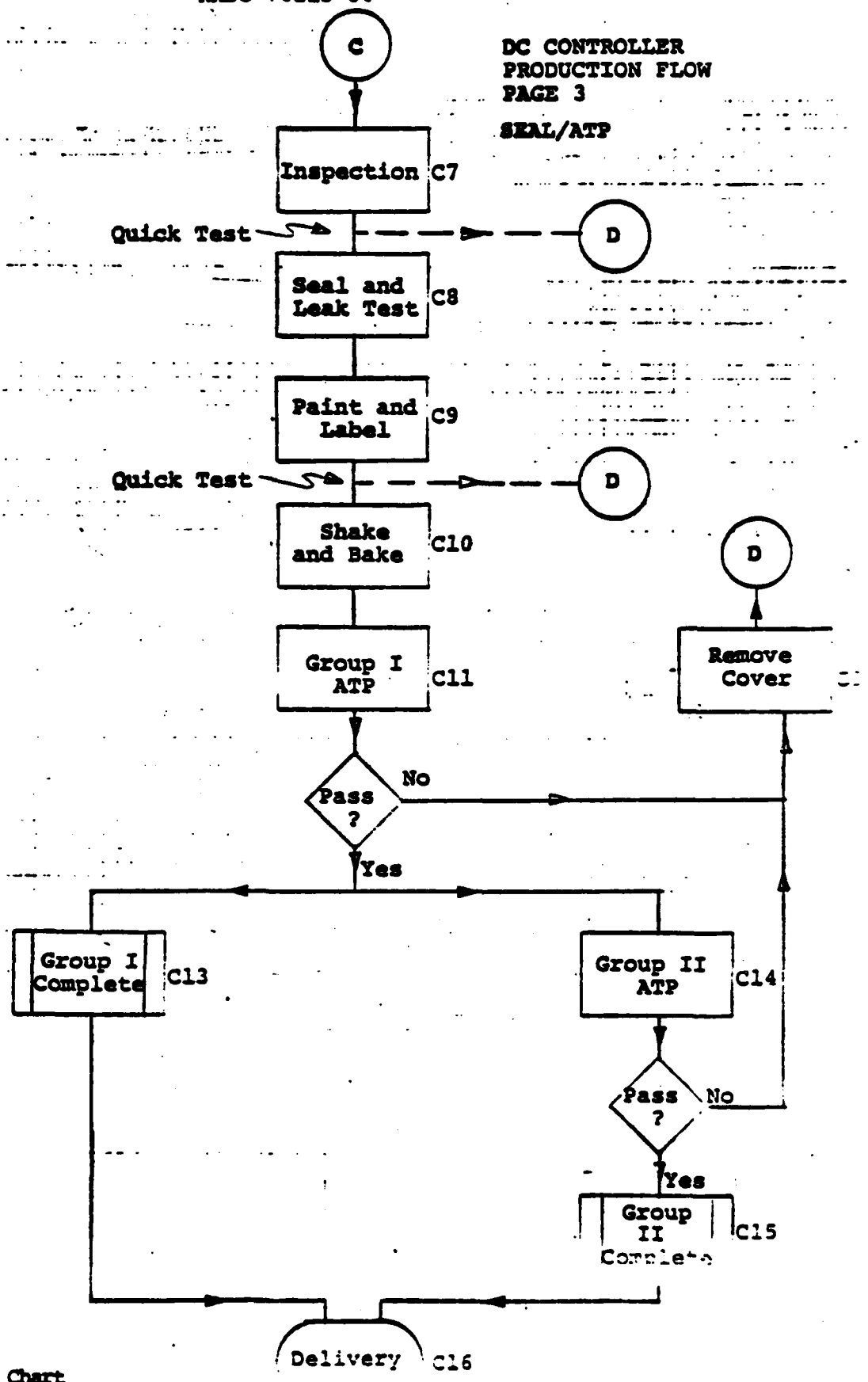


Fig. 14c
Production Flow Chart

Incorporated as part of the procedures, all hybrids were visually inspected to detect abnormalities prior to being powered up. Since both logic and amplifier substrates require active trimming to bring operational tolerances within limits, rudimentary tests (L3 and A3) were performed to exercise those components affected by dynamic trimming. The test point measured during the trim procedure was recorded at the trim facility and remeasured after trimming at the evaluation test position. This would detect differences in instrumentation between the two work positions.

After trimming, the amplifier hybrid was checked for proper operation at 17.5V and 30V. Supply current was measured to determine maximum power dissipation. The output of the trip time integrator, the minimum current detector and the gain compensation amplifier were checked by simulating the voltage developed across the current sensing resistor. The rise/fall time amplifier was checked by connecting the inputs to a DC potential and measuring for a fixed output voltage.

The logic hybrids were evaluated fcr the stability of the on-board voltage regulator, correct operation of the combinational logic elements, power dissipation, proper Zener diode voltage and switching capability of the input circuit transistors. Signal timing is not incorporated as part of the hybrid evaluation test.

Hybrids that did not comply with the established standards were evaluated to determine the nature of the failure and, if

possible, the fault was corrected and the hybrid was retested. Faults that were typically detected at this stage would be defective IC's, out of value resistors and damaged wire bonds. After completing the hybrid tests and passing QC inspection, the control subassembly was constructed. Three opto-couplers that had previously been tested at 125°C for transfer characteristics and switching speed are attached to the two back-to-back substrates.

4.2 Power Subassembly

The power hybrid construction started with the printing of the copper backplane, copper conductor traces and an insulating ink onto the BeO substrate.

The substrate was populated in multiple steps, using different temperature solders. First, the posts used to hold the power transistor clips were attached to the substrate, using Au Ge solder at 400°C in a hydrogen atmosphere. Then the power output transistor and its base and emitter clips were attached, using solder preforms at 330°C in a reducing H_2N_2 atmosphere.

At this stage, the power transistors were tested for leakage current. If a stage was found defective on a substrate mounted with multiple output stages, the hybrid would be downgraded in current rating. Therefore, two stages of 10A power hybrid could be disabled by removing the transistor clips, thus forming a 5A unit. Similarly, the defective stage of a designated 5A unit could be disabled and the substrate could be used for a 2A or 1/2A controller.

At this point, the lower power transistors and diodes were epoxied to the substrate and cured. All semiconductors were then wire bonded with gold wire. The transistor terminals that would be required to pass high current were connected with multiple bond wires.

The final population step was to solder the pretrimmed chip resistors to the substrate. The resistor values selected would be determined by the rating of the power hybrid. Prior to assembly of hybrid to header, the epoxy insulation was tested, placing the hybrid on a wet blotter situated on the metal plate and applying the 1000V RMS test voltage between the plate and each pin. Having passed this test, the hybrid and header were soldered together.

The power hybrid was tested after being mounted to the header baseplate. Prior to power up, the unit was given a visual examination and the subassembly serial number was assigned.

The assembly was checked with 1000V AC for dielectric isolation. Off-state leakage current was checked by derating the specification values given at 100°C to projected currents at 25°C. The output stage was tested at the current rating of the controller that it would be assembled into. The voltage drop across the output stage was also measured at the rated current. The gain compensation control circuitry was also exercised to insure that it would deliver adequate drive current.

4.3 Controller Integration

At the pre-cap stage, the control subassembly (logic and amplifier hybrids plus the three opto-couplers) was press-fitted on top of the power subassembly and temporary riser wires were attached between the two levels. Since this was the first time that all components interact completely within the particular controller module, tests were performed to insure proper operation within specification limits. Isolation, insulation resistance, and dielectric withstanding high voltage tests were not performed at this stage since the controller circuitry was still exposed to a possibly humid ambient environment. Transient tests were also not exercised during pre-cap evaluation since the controller response to transients was mostly dependent on design and not component interaction variations. The only other test not performed at the pre-cap stage was the trip time characteristics at output currents above 150%.

In the event that the controller had failed any test at the pre-cap stage, the unit could be debugged while still assembled. The control assembly could easily be removed for repair at this stage since all electrical and mechanical connections were only of a temporary nature. If necessary, the logic and amp. hybrids could be separated, but most repairs could be made with the two hybrids back-to-back. After repair, the controller was, again, subjected to the pre-cap test phase.

After the controller passed the pre-cap test phase, the control subassembly was permanently soldered onto the support pins, and riser wires from the power subassembly to the upper level were permanently attached. It had been observed that some of the controllers had trip BIT voltages that were marginal or slightly below the specification limits when examined at the pre-cap test level. It was determined that an active trim to R2 on the exposed logic hybrid could easily be performed to pull the trip response level to the center of acceptable limits. This conditional step is shown at Block C6 on Figure 14b.

Prior to inspection at C7, the opto-couplers were epoxied to the logic hybrid for additional support. After inspection, but prior to having the cover attached, the integrated assembly was subjected to a quick series of tests to confirm that no damage occurred during the final solder, trim or epoxy operations. The header cover was then fitted and soldered in place, the unit was purged, baked, and backfilled with dry nitrogen prior to sealing the tip-off port. The controller was then tested for seal integrity as outlined by the specification and as part of the Acceptance Test Procedure. The serial number assigned to the controller at this point was the manufacturing line number that was used on its power subassembly.

The sealed controllers were then mounted on a plate, to cover their heat sink surface. The units were then sprayed with black epoxy paint.

The first thirty-one controllers constructed were then subjected to vibration of 2.5 G's at 55 Hz at temperature extremes of -30°C and +85°C. The period of vibration lasted ten minutes at each extreme after temperature stabilization. Although this processing step was not a contractual requirement, it was determined that this stress cycle would insure confidence in the mechanical integrity of the construction.

Since problems did not become evident due to the shake and bake cycle, this processing step was eliminated for the remaining controllers. The controllers then proceeded to final testing.

4.4 Controller Testing

After the final assembly step, the controllers were evaluated for compliance with Specification NO. NADC-30-TS-7602 dated 27 April 1976. This was performed in accordance with contract requirements and applicable specification items for DC controllers. All 100 controllers were checked against the appropriate items listed in Group I, Table III of the specification. Three controllers of each rating were additionally checked against the appropriate requirements of Group II and Group III of Table III. These controllers were not required to be tested for temperature shock, acceleration, salt fog, or humidity as per the contract. In addition, it was agreed upon that NADC would perform vibration, temperature altitude, radio interference, shock and life tests.

4.4.1 Group I Test Procedure

The test procedure given in Appendix C was adopted to check each controller's compliance, with the specifications. Each test

paragraph lists the title of the step being performed, the Requirements and Quality Assurance Provisions references to specification Paragraphs 3 and 4, and any applicable definitions given in Section 6.5. The test paragraph also includes an explanation of the procedure to be performed at that test step and the acceptable limits allowed.

The initial tests performed on a controllers checked the high voltage isolation between the terminal and case and between the control input circuitry and the components tied to the power terminals. The controller was then connected to a heat sink test fixture.

The Power Input terminal was connected to a 30V, 80A power supply and the Power Output terminal was connected to the appropriate load via soldered wire connections. The Power Ground, Control Input, and Control Ground connections were made with clip-on leads and fed to the test control box. In addition, clip leads were attached to the Power Input and Power Output terminals so that voltage measurements could be made directly on the controller without the effects of the resistance of the power lead wires.

The control and measurement leads were fed to a test control box that contained a rotary switch for convenient measurement between the various test points, and a set of voltage comparators used for the accurate measurement of the power output rise, fall and delay times. The outputs of the voltage comparators were fed into gating logic whose outputs represented controller waveform times and were selected via a rotary switch to feed an interval

timer. The schematic of the test box referred to in the test procedure is shown in Figure 15.

4.4.2 Group I Test Results

The test procedure given in Appendix C includes both quantitative and qualitative criteria used to examine each controller. The procedure also includes the set-up steps to be taken before making measurements and remeasurements taken to confirm proper operation after severe tests were performed. The quantitative measurements of the controller characteristics are shown in Table 1. Each column of data represents a numbered step in the test procedure. Test steps in which data is not given in the table are explained below.

Steps 1 and 2 confirm the mechanical characteristics of the controller at the time of testing.

Step 3 assures that the hermetisity requirement of the specification was met. All controllers were tested for, and passed a fine leak requirement of a leakage rate of less than 10^{-6} $\frac{\text{ATM-CC}}{\text{SEC.}}$. All controllers also passed the gross leak test in which no escaping bubbles were observed when the controller was soaked in hot freon.

All controllers passed the di-electric withstanding voltage of 1000V AC RMS of Step 4 without breakover.

All controllers had leakage currents less than 1u amp when 100V was applied between the points outlined in Steps 5 and 6. This is equivalent to isolation and insulation resistances greater than 100MΩ for these tests.

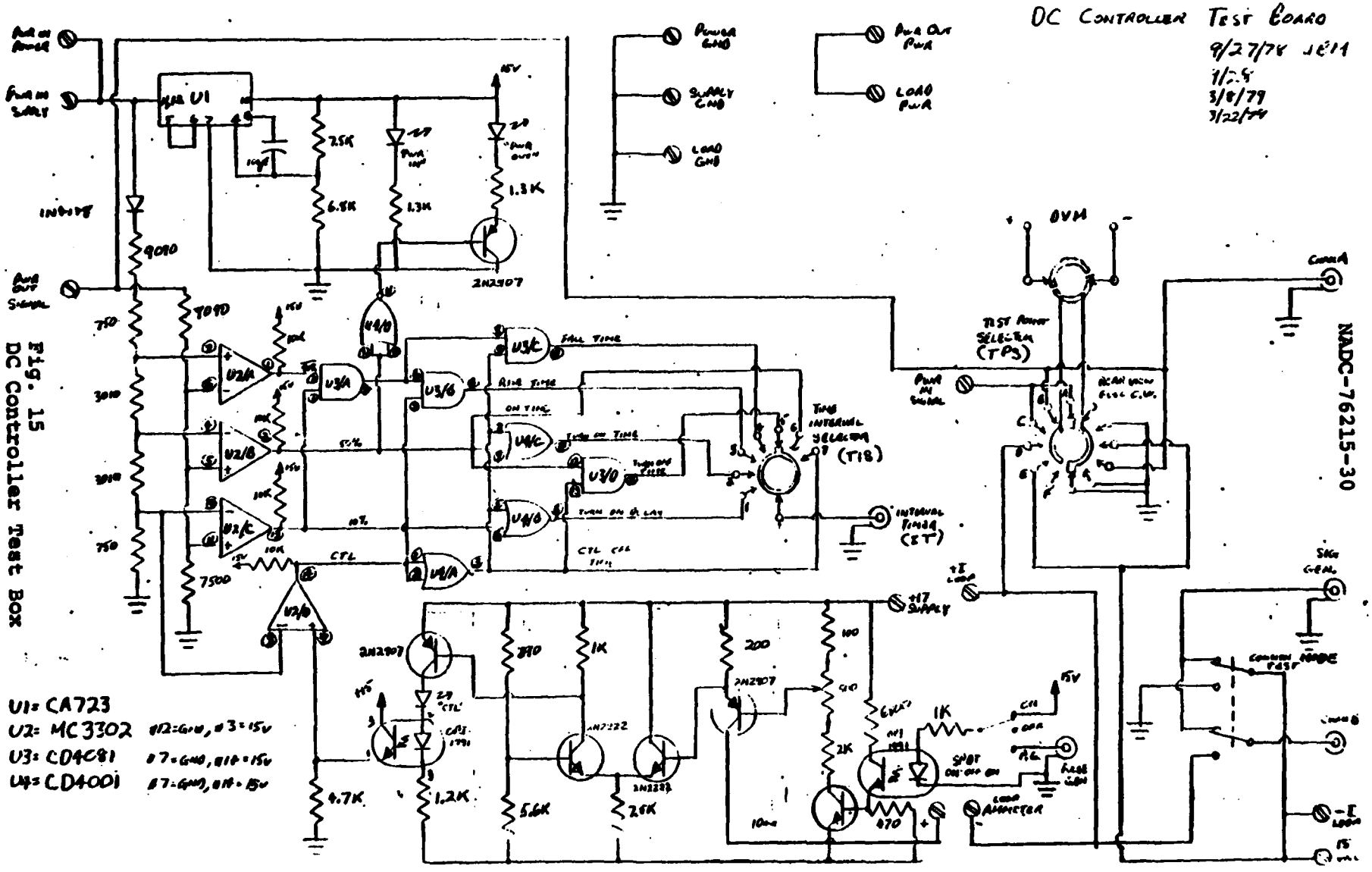


Fig. 15
DC Controller Test Box

Table 1. Group I test results.

SER.#	TEST NO. / RATING	10 ms	11 ms	12 ms	13 ms	14 ms	15 mA	16 mA	17 V	18 µs	19 V	20 W	21 W	22 µA	24 Ω	25 ms	26 ms	27 ms	31 V	35 V	40 µs
3	10	.47	.54	.15	.33	1.58	.88	1.14	6.79	16	.94	11.31	.23	<1	3.67	166	103	.3	4.19	10.8	6
7	10	.45	.51	.14	.32	1.44	.9	1.2	7.15	18	.93	11.34	.22	<5	6.2	164	1	.2	4.1	11.0	
8	10	.42	.48	.13	.32	1.46	.88	1.12	6.85	20	.94	11.44	.24	<1	3.1	144	86	.4	4.19	10.9	6.5
9	10	.41	.48	.13	.31	1.40	.95	1.27	6.89	17	.93	11.30	.22	<5	3.3	152	95	.2	4.21	10.83	
20	10	.45	.52	.15	.31	1.39	.94	1.24	6.96	16	.95	11.78	.23	<1	3.03	159	80	.3	4.18	10.95	7
22	10	.44	.50	.14	.29	1.34	.93	1.23	7.03	16	.94	11.41	.23	<1	3.85	169	80	.3	4.19	11.06	6
23	10	.41	.47	.13	.34	1.55	.87	1.17	6.99	23	.93	11.55	.23	<1	4.6	168	83	.3	4.12	10.98	
24	10	.45	.52	.14	.33	1.48	.83	1.14	6.85	20	.93	11.28	.23	<1	3.6	160	80	.4	4.08	10.82	
26	10	.45	.51	.14	.32	1.43	.92	1.23	6.94	22	.94	11.92	.23	<1	2.4	165	77	.5	4.16	10.9	
32	10	.41	.48	.15	.35	1.44	.89	1.19	6.91	15	.95	11.0	.24	<1	2.6	167	80	.35	4.13	10.9	6
98	10	.46	.53	.145	.33	1.47	.93	1.22	6.95	16	.935	11.84	.26	<1	2.88	164	94	.35	4.02	10.98	6
99	10	.46	.47	.02	.04	1.64	.90	1.18	6.74	17	.90	11.2	.25	<1	1.95	146	84	.19	4.29	10.78	6
160	10	.47	.53	.13	.27	1.35	.88	1.18	7.70	14	.955	11.65	.26	<2	2.12	164	85	.25	4.03	11.48	6

TABLE 1. Group I Test Results.

SER.#	TEST NO. / RATING	10 ms	11 ms	12 ms	13 ms	14 ms	15 mA	16 mA	17 V	18 ms	19 V	20 W	21 W	22 μA	24 s	25 ms	26 ms	27 ms	31 V	35 V	40 μs
14	5	.39	.45	.12	.33	1.49	.93	1.21	6.62	17	.92	7.6	.23	<1	2.78	153	61.1	.25	4.21		6
15	5	.46	.54	.15	.33	1.48	.95	1.25	6.80	16	.91	6.1	.22	<1	3.88	166	90	.28	4.17	10.8	6
28	5	.45	.52	.14	.30	1.39	.98	1.30	6.76	15	.94	6.1	.22	<1	4.29	160	82	.25	4.12	10.77	6
29	5	.43	.49	.14	.33	1.53	.92	1.24	6.98	18	.95	6.16	.22	<1	2.44	162	85	.27	4.15	10.87	6
86	5	.419	.472	.112	.318	1.7	.73	1.1	7.89	14	.94	6.26	.24	<1	3.05	153	47	.33	4.11	11.7	5
87	5	.48	.55	.136	.30	1.43	1.01	1.31	7.32	15	.947	6.33	.24	<1	6.80	150	83	.25	4.21	11.70	6
89	5	.46	.53	.14	.30	1.39	.92	1.23	7.81	12	.94	6.14	.24	4	4.05	170	88	.2	4.04	11.55	5
92	5	.47	.53	.14	.31	1.42	1.01	1.40	7.54	14	.94	6.14	.24	<1	3.41	167	80	.23	3.91	11.35	5
93	5	.63	.66	.14	.31	1.66	.92	1.07	7.36	15	.95	6.28	.24	<1	4.02	170	90	.3	4.05	11.60	5
94	5	.46	.52	.137	.29	1.37	1.01	1.31	6.98	16	.946	6.17	.24	<1	3.90	146	54	.39	4.19	10.93	6
95	5	.48	.55	.15	.31	1.34	1.13	1.53	6.91	15	.95	6.19	.24	<1	3.21	167	82	.25	4.11	10.86	6
128	5	.518	.590	.150	.328	1.507	1.22	1.40	7.06	12	.960	6.48	.261	<1	4.97	178	95	.2	4.58	10.15	6
129	5	.47	.53	.138	.31	1.44	.84	1.09	7.75	13	.938	6.31	.27	15	5.50	178	92	.41	4.57	11.51	5
131	5	.47	.53	.138	.30	1.37	.91	1.21	6.87	14	.94	6.18	.24	<1	2.09	142	41	.26	4.04	10.83	5
153	5	.49	.56	.146	.317	1.50	.86	1.12	7.30	14	.966	6.27	.24	<1	2.70	154	32	.24	3.90	11.07	6
156	5	.49	.56	.138	.29	.137	.84	1.10	7.43	14	.985	6.40	.24	<1	2.55	142	84	.21	3.88	11.25	6

TABLE 7. Group I Test Results.

SER.#	TEST NO. / RATING	10 ms	11 ms	12 ms	13 ms	14 ms	15 mA	16 mA	17 V	18 µs	19 V	20 W	21 W	22 µA	24 Ω	25 ns	26 ns	27 ns	31 V	35 V	40 µs
62	2	.43	.48	.121	.35	1.58	.88	1.18	7.82	14	.855	.996	.26	<1	5.49	215	112	.38	4.60	11.63	5
63	2	.51	.58	.153	.31	1.43	.85	1.11	6.60	17	.919	2.68	.26	<1	2.65	175	88	1.4	4.33	10.63	6
64	2	.51	.58	.15	.32	1.52	.84	1.09	6.87	15	.93	2.64	.23	<1	3.60	165	85	.25	4.20	10.85	5.3
66	2	.46	.53	.14	.30	1.37	1.20	1.22	6.64	16	.93	2.65	.21	<1	4.03	170	81	.3	4.24	10.59	6
70	2	.45	.51	.14	.31	1.38	1.04	1.36	6.84	16	.948	2.46	.24	2	2.03	164	84	.25	4.16	10.82	5
85	2	.50	.57	.146	.31	1.45	.91	1.21	7.06	16	.919	2.43	.24	<1	4.03	167	84	.28	4.24	11.05	6
101	2	.50	.57	.141	.82	1.44	.82	1.03	7.34	18	.925	2.66	.25	<1	7.26	173	88	.3	4.27	11.2	5.5
102	2	.47	.53	.13	.28	1.37	.78	1.02	7.05	17	.925	2.46	.25	<1	3.55	167	83	.25	4.16	11.0	6
104	2	.50	.56	.139	.29	1.49	.72	.90	7.23	17	.922	2.45	.25	<1	5.23	190	95	.3	4.10	11.03	7
107	2	.47	.56	.139	.31	1.43	1.01	1.29	7.37	15	.936	2.71	.25	<1	2.66	166	79	.29	3.86	11.24	5
108	2	.51	.58	.153	.31	1.44	.90	1.16	6.79	17	.929	2.67	.24	<1	3.39	187	89	.4	4.11	10.75	5
109	2	.49	.56	.137	.29	1.39	.90	1.15	7.59	15	.944	2.73	.25	<1	2.57	165	83	.27	4.48	11.42	5
112	2	.46	.53	.140	.33	1.51	.94	1.21	6.82	17	.952	2.68	.23	<1	4.67	181	98	.32	4.13	10.79	6
113	2	.49	.57	.155	.32	1.42	.97	1.29	6.91	16	.943	2.70	.22	<1	2.19	197	85	.32	4.26	10.86	6
114	2	.48	.54	.140	.30	1.38	.99	1.29	7.76	13	.933	2.68	.25	<1	2.68	182	91	.28	4.07	11.6	5
115	2	.49	.56	.141	.30	1.38	.91	1.18	7.30	13	.944	2.70	.25	<1	4.13	188	94	.28	4.33	11.16	6
119	2	.47	.54	.134	.28	1.35	.90	1.18	7.52	7	.923	2.96	.26	<1	2.81	179	88	.3	3.97	11.35	6
122	2	.47	.54	.132	.28	1.35	.87	1.09	7.70	17	.927	2.69	.26	<1	7.00	196	97	.31	4.56	11.50	5
123	2	.47	.54	.160	.36	1.45	.98	1.28	7.74	13	.931	2.67	.25	<1	3.28	197	98	.32	4.61	11.47	6
125	2	.46	.52	.131	.29	1.38	.88	1.14	6.97	16	.933	2.65	.23	<1	3.17	179	94	.34	4.10	10.7	6
126	2	.37	.43	.130	.43	1.63	.90	1.22	6.88	16	1.01	2.84	.25	<1	4.87	182	87	.63	4.45	10.9	6

TABLE 1. Group I Test Results.

SER.#	TEST NO. / RATING	10 ms	11 ms	12 ms	13 ms	14 ms	15 mA	16 mA	17 V	18 μs	19 V	20 V	21 V	22 μA	24 s	25 ms	26 ms	27 ms	31 V	35 V	40 μs
5	2	.50	.58	.15	.29	1.38	.83	1.13	7.38	19	.93	2.68	.24	<1	6.03	189	88	.2	4.23	10.80	6
13	2	.5	.57	.15	.28	1.33	.88	1.16	7.1	20	.92	2.64	.23	<1	6.33	198	97	.3	4.09	11.13	6
35	2	.47	.54	.15	.30	1.39	.92	1.22	6.9	23	.93	2.65	.23	<1	1.53	161	84	.32	4.24	10.9	6
36	2	.47	.53	.13	.27	1.31	.95	1.28	7.0	17	.94	2.69	.24	<1	1.38	152	80	.25	4.14	11.04	6
38	2	.47	.54	.14	.30	1.45	.92	1.19	6.76	15	.92	2.65	.24	<1	3.31	152	79	.25	4.12	10.75	6
39	2	.46	.52	.13	.29	1.38	.85	1.12	6.71	15	.93	2.65	.21	<1	3.51	168	83	.35	4.06	10.5	5.5
40	2	.47	.54	.14	.31	1.39	1.01	1.32	6.70	15	.93	2.67	.26	1	1.90	162	83	.3	4.10	10.67	5
41	2	.50	.57	.14	.29	1.36	.98	1.24	6.76	14	.93	2.64	.23	2	4.39	170	80	.26	4.18	10.77	6
44	2	.48	.55	.14	.28	1.34	.92	1.18	6.58	18	.93	2.64	.24	<1	2.61	153	78	.21	4.10	10.60	6
45	2	.46	.52	.14	.29	1.32	.85	1.10	6.68	16	.92	2.64	.24	<1	1.75	152	72	.3	4.11	10.68	6
46	2	.45	.52	.14	.32	1.43	.93	1.23	6.72	16	.91	2.64	.25	<1	4.85	186	100	.25	4.17	10.7	15
47	2	.44	.50	.13	.27	1.26	.88	1.12	6.87	15	.92	2.67	.26	<1	2.49	154	83	.3	4.18	10.88	6
48	2	.49	.56	.14	.30	1.29	.93	1.19	6.92	13	.93	2.61	.24	<1	5.84	185	95	.4	4.19	10.97	6
51	2	.47	.53	.13	.27	1.34	.92	1.19	6.95	15	.97	2.74	.24	<1	2.91	176	87	.24	4.20	10.84	7
53	2	.45	.52	.134	.29	1.36	.70	.95	6.95	16	.936	2.47	.27	<1	3.97	181	95	.39	3.97	10.95	6
54	2	.50	.57	.150	.32	1.47	.86	.99	6.78	16	.921	2.71	.25	<1	3.04	168	83	.21	3.80	10.39	6
56	2	.48	.54	.14	.28	1.38	.99	1.28	6.62	16	.92	2.65	.24	<1	4.15	154	77	.29	4.20	10.62	5
57	2	.495	.664	.146	.311	1.434	.98	1.23	6.88	13	.933	2.67	.242	<1	3.69	181	95	.3	4.10	10.80	6
58	2	.49	.56	.14	.33	1.38	.91	1.23	6.54	15	.94	2.58	.24	1	2.41	158	80	.32	4.45	10.54	7
59	2	.50	.57	.15	.32	1.47	.93	1.20	6.58	16	.92	3.19	.23	1	4.37	168	81	.25	4.16	10.6	6

TABLE 1. Group I Test Results.

TEST NO. / REF.	RATING	10 mm	11 mm	12 mm	13 mm	14 mm	15 mA	16 mA	17 V	18 mm	19 V	20 V	21 W	22 mA	24 Ω	25 mm	26 mm	27 mm	31 V	35 V	40 mm
130	2	.48	.55	.14	.30	1.40	.88	1.12	7.75	14	.93	2.68	.25	1	3.15	197	99	.38	4.55	11.59	5
132	2	.48	.55	.144	.31	1.37	.90	1.18	6.82	16	.93	2.69	.24	<1	3.44	174	88	.32	4.20	10.8	6
134	2	.47	.54	.14	.28	1.34	.86	1.10	6.84	15	.95	2.71	.24	<1	3.76	195	98	.28	4.05	10.75	6
144	2	.44	.49	.12	.29	1.39	.98	1.32	6.63	16	.947	2.73	.25	<1	3.21	189	91	.30	4.1	10.64	6
150	2	.47	.54	.137	.29	1.36	.88	1.26	7.01	16	.94	2.72	.24	<1	3.25	191	96	.29	4.25	11.07	6.5

	TEST NO.	10	11	12	13	14	15	16	17	18	19	20	21	22	24	25	26	27	31	35	40
SER. #	RATING	ms	ms	ms	ms	ms	mA	mA	V	μs	V	W	W	μA	s	ms	ms	ms	V	V	μs
10	½	.41	.47	.12	.28	1.39	.83	1.20	6.84	17	.85	.97	.23	<1	4.80	182	97	.08	4.22		
12	½	.45	.51	.13	.30	1.57	.86	1.17	6.87	15	.85	.97	.23	<1	3.9	142	75	.33	4.12	10.98	6
17	½	.46	.53	.15	.35	1.55	.89	1.21	6.72	15	.86	.99	.24	<1	2.77	178	92	.27	4.06	10.73	6
67	½	.45	.52	.14	.33	1.54	.86	1.15	7.04	11	.87	.98	.23	<1	2.53	169	89	.28	4.02	11.00	5
69	½	.43	.48	.121	.35	1.58	.88	1.18	7.82	14	.855	.9975	.24	<1	5.49	215	112	.38	4.60	11.63	5.6
71	½	.47	.53	.130	.32	1.49	.93	1.21	7.70	19	.856	.998	.24	<1	2.30	162	86	.2	4.58	11.52	6
72	½	.45	.51	.136	.32	1.48	.88	1.14	6.81	14	.849	1.02	.26	1	3.85	170	86	.21	4.14	10.79	6
73	½	.44	.50	.128	.28	1.53	.81	1.10	6.96	15	.847	1.01	.25	<1	2.34	174	82	.35	4.08	11.07	5
74	½	.44	.49	.120	.26	1.48	.89	1.22	7.04	16	.848	1.009	.26	<1	3.67	168	85	.27	4.12	11.01	8
75	½	.45	.49	.11	.27	1.51	.84	1.27	6.94	17	.85	.995	.21	<1	3.92	172	87	.3	4.33	10.93	7
76	½	.46	.52	.128	.29	1.49	.86	1.16	7.05	15	.854	.997	.23	<1	3.09	176	92	.23	4.14	10.93	6
78	½	.41	.46	.11	.25	1.38	.79	1.08	6.89	15	.85	.97	.22	<1	3.77	179	92	.29	4.21	10.86	6
79	½	.44	.50	.13	.30	1.45	1.01	1.33	6.83	17	.85	.98	.24	<1	3.0	174	85	.3	4.14	10.8	6
80	½	.46	.53	.13	.28	1.41	.95	1.23	6.74	15	.84	.98	.24	<1	8.74	172	87	.19	4.16	10.7	6
81	½	.45	.51	.13	.29	1.47	.89	1.21	7.19	14	.86	.99	.24	<1	5.03	161	89	.23	4.18	11.1	5.5
82	½	.45	.51	.14	.29	1.48	.96	1.27	6.72	15	.86	1.015	.25	<1	4.30	175	87	.25	4.0	10.7	6
83	½	.434	.495	.123	.307	1.43	.92	1.21	7.12	14	.856	1.057	.276	<1	1.99	155	79.6	.24	3.99	11.25	5
84	½	.43	.48	.113	.24	1.39	.99	1.27	6.91	15	.854	.997	.24	<1	4.37	176	94	.25	4.11	10.95	6
90	½	.46	.52	.126	.29	1.60	.85	1.10	7.53	14	.84	.996	.24	<1	4.14	192	92	.27	4.45	11.39	5

TABLE 1. Group I Test Results.

TABLE 1. Group I Test Results.

SER.#	TEST NO. RATING	10 ms	11 ms	12 ms	13 ms	14 ms	15 mA	16 mA	17 V	18 μs	19 V	20 V	21 V	22 μA	24 s	25 ms	26 ms	27 ms	31 V	35 V	40 μs
121	½	.42	.48	.133	.34	1.53	.86	1.16	6.86	15	.846	1.03	.26	<1	3.25	184	95	.22	4.26	10.95	7
139	½	.46	.52	.124	.3	1.50	.84	1.08	6.78	14	.849	.995	.24	<1	6.26	205	102	.22	4.20	10.65	6
143	½	.44	.50	.126	.27	1.47	.95	1.23	7.02	13	.86	1.03	.26	<1	3.81	209	101	.25	4.19	10.91	5
145	½	.43	.49	.12	.26	1.37	.94	1.21	6.78	16	.86	1.00	.26	<1	2.79	194	95	.25	4.17	10.7	6
146	½	.46	.52	.12	.26	1.42	1.0	1.29	7.54	13	.86	.998	.26	<1	3.68	202	100	.22	4.4	11.4	5
148	½	.46	.53	.14	.32	1.56	.90	1.18	6.82	15	.86	1.05	.28	2	2.73	183	94	.26	4.32	10.8	6

Steps 7, 8, and 9 are set-up and run-in procedures used to assure proper operation before quantitative data was taken.

Steps 10 to 22 results are listed in Table 1.

Step 23 is a set-up and calibration step used in preparation for the trip time tests.

Steps 24 to 27 results are listed in Table 1.

Steps 28 and 29 are consequences of successful completion of all trip time tests.

All controllers would not reset when a 4.5m sec. turn off pulse was applied in Step 30.

Step 31 results are listed in Table 1.

For Step 32, all controllers had an observed AC voltage drop of less than .01 volts with most units reading about .001 volts AC. This can be related to the ripple current developed by the controller into a resistive load. This test was performed only at rated output current since the controller design did not include AC developing circuitry.

Prototype tests indicated that controllers would not produce a ripple current at any intermediate load current.

All controllers tested passed the common mode rejection test of Step 33.

For Step 34, all controllers were forced to a Fault/Bit impedance and the input current was adjusted to the point where the voltage between the input terminals was 15V. Since the required input current to obtain this voltage was approximately 14 ma., maximum power was applied to the input circuitry without exceeeding the maximum voltage or current specifications. Proper operation of the control input circuitry after testing is measured in Steps 35 to 40.

Step 35 results shown in Table 1.

Steps 36, 37, and 38 remeasure controller characteristics to assure proper operation after trip time and maximum control signal tests.

Step 39 remeasures the Bit/Fault level taken in Step 35 under a different Fault condition. All controllers had the same Bit levels for both Steps 35 and 39.

Step 40 results shown in Table. (This test step was not included in the original test procedure; because of this, some of table entries are missing.)

4.4.3 Group II and Group III Test Results

Three controllers of each rating was tested for the applicable items of Table III, Group II and Group III of the specification, after passing Group I tests. Included in this group were the Operating Voltage Transient and Transient Spike Overvoltage tests

applied to the power terminals of the controller plus the control input transients applied to the control terminals.

All twelve units were also tested at temperature extremes of -54°C and 120°C, as measured on heat sink to which the controller was attached. The test procedure that was used for Group I testing was also used to test operation at temperature extremes, but with the test sequence starting at Step 7. (See Appendix C for test procedure.) Test results of measurements made at -54°C and 120°C are given in Table 2.

After being tested at temperature extremes, the controllers were then each tested at room temperature for proper operation after operating voltage transients and transient overvoltage spikes were applied to the power terminals and control input transients were applied to the control terminals. Proper operation was assured by testing each unit for compliance with the applicable items of Table IV, Group A of the Specification.

It was observed that the controller output would turn on for 2 to 3 milliseconds when the control transient pulse train was applied. This was determined to be caused by the integration of the pulse train by the opto-coupler Z3 and delay time integrator R11 and C1. Since the delay before turn is allowed to be as short as 100μ sec. and the delay before turn off as long as 2.0m sec., it was determined that this duration turn on short was not a violation of the specification.

TABLE 2. Test Results - Operation at Temperature Extremes.

SER. #	TEST NO. / RATING (°C)	10 ms	11 ms	12 ms	13 ms	14 ms	15 mA	16 mA	17 V	18 µs	19 V	20 W	21 W	22 µA	24 s	25 ms	26 ms	27 ms	31 V	35 V	40 µs
3	10 (-55)	.64	.74	.21	.26	1.10	.65	.89	6.70	.12	1.057	12.01	.25	<1	4.48	171.3	89.6	.45	4.32	10.62	6
	(+120)	.31	.37	.13	.58	2.1	1.2	1.59	7.00	40	.82	10.18	.20	57	1.52	135	72.8	.6	4.2	10.9	25
8	10 (-55)	.56	.64	.17	.24	1.08	.68	.94	6.63	10	1.04	12.47	.27	<1	5.59	142	94	.375	4.25	10.60	4.5
	(+120)	.28	.32	.10	.53	1.84	1.24	1.61	7.07	33	.81	11.05	.21	<1	1.45	123	70	.52	4.17	11.23	33
9	10 (-55)	.57	.66	.18	.24	1.05	.7	.93	7.00	5	1.05	12.36	.25	<1	5.94	171	88.9	.4	4.42	11.02	6
	(+120)	.29	.34	.104	.52	1.80	1.42	1.84	6.82	35	.82	9.18	.1999	55	1.82	142	50	.6	4.03	10.8	30
88	5 (-55)	.61	.70	.19	.22	.95	.58	.80	7.60	8	1.066	6.5	.27	<1	10.9	191	98	.7	4.13	11.329	4
	(+120)	.31	.56	.114	.51	1.80	1.44	1.80	8.02	28	.821	5.51	.218	76	2.19	147	80	.3	4.02	11.76	15
92	5 (-55)	.61	.71	.195	.23	.998	.75	1.03	7.51	7	1.08	6.54	.263	<1	10.01	172	87	.42	4.15	11.21	4.5
	(+120)	.30	.36	.11	.49	1.79	1.46	1.86	7.65	27	.82	5.48	.24	87	2.08	136	68	.4	3.79	11.47	20
93	5 (-55)	.76	.85	.19	.24	1.24	.61	.70	7.6	10	1.09	7.07	.27	<1	19.22	162	85	.4	4.51	11.00	5
	(+120)	.41	.46	.12	.52	2.1	1.24	1.48	7.16	33	.83	5.71	.22	55	1.32	122	48	.5	3.74	10.86	30
40	2 (-55)	.57	.66	.18	.23	1.00	.81	1.11	6.74	90	1.07	3.00	.28	<1	3.54	182	95	.32	4.27	10.75	5
	(+120)	.31	.38	.13	.52	1.82	1.45	1.94	6.72	33	.78	2.37	.21	77	1.21	135	72	.42	3.98	10.6	30
56	2 (-55)	.61	.69	.18	.22	.99	.75	1.02	6.40	10	1.05	2.95	.28	<1	21	184	87	.33	4.26	10.3	5
	(+120)	.32	.38	.13	.47	1.83	1.52	1.94	6.9	32	.78	2.37	.24	29	1.88	132	65	.41	4.24	10.93	30
64	2 (-55)	.62	.71	.19	.25	1.12	.67	.89	6.67	10	1.06	2.97	.29	<1	17	179	90	.6	4.26	10.66	4
	(+120)	.32	.39	.14	.56	2.01	1.14	1.56	7.05	30	.78	2.37	.24	21	1.65	143	70	.5	4.15	10.93	20
75	.5 (-55)	.53	.61	.14	.21	1.08	.67	.95	6.76	10	1.00	1.07	.24	<1	11.27	198	93	.33	4.39	10.72	5
	(+120)	.29	.33	.100	.57	2.1	1.44	2.0	7.2	60	.67	.89	.20	437	2.00	147	76	.7	4.3	11.1	30
79	.5 (-55)	.53	.61	.16	.24	1.05	.76	1.09	6.61	11	1.00	1.07	.25	<1	18.7	193	95	.32	4.19	10.5	5
	(+120)	.30	.35	.104	.60	2.07	1.45	1.95	7.13	55	.67	.86	.21	25	1.89	145	75	.9	4.17	11.1	33
80	.5 (-55)	.56	.63	.15	.21	1.02	.69	.97	6.55	9	.997	1.07	.26	<1	7.93	1710			4.26	10.5	5
	(+120)	.31	.36	.105	.53	1.98	1.52	1.92	7.01	32	.66	.87	.21	49	3.14	142	73	.6	4.15	10.9	33

4.4.4 Bit Fault Tests

One controller was specially constructed so that the Bit/Fault condition simulating a shorted power output transistor could be tested in accordance with Table III, Group III of the specification. This controller (#83, 1/2A) had an additional wire attached to the emitter of the power output transistor. The wire was then fed through a hole in the plexiglas cover that was used in place of the metal header cover. The controller was then tested for electrical compliance with the specification with the exclusion of the high voltage isolation tests. This unit was then tested in a normal condition with a 10m sec wide 10ma pulse turning the output on as shown in Figure 16a. The wire attached to the emitter of the output transistor was then shorted to the power output terminal to simulate a shorted output transistor with the results as shown in Figure 16b. Note that the initial Bit response indicates a Fault condition (11V control input voltage) since the controller was passing output current directly before the input signal was applied. The Bit response then reverts back to the normal level. (7.2V control input voltage) since there is, at that time, a control signal to turn on and the controller is passing rated load current. Figure 16c shows the controller's fault response to a 50μ sec. interrogation on an expanded time scale. Figure 16d indicates the Normal Bit input response with an interrogation pulse when the simulated fault was removed.

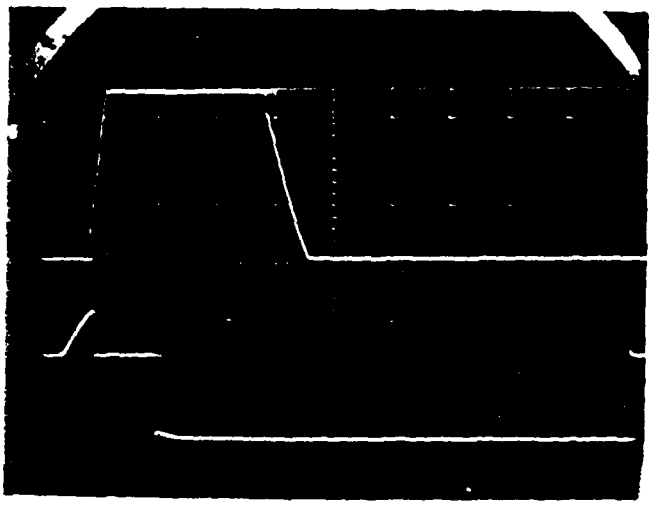


Figure 16a. Normal Operation with 1 ms Turn on Pulse Every 5 ms.

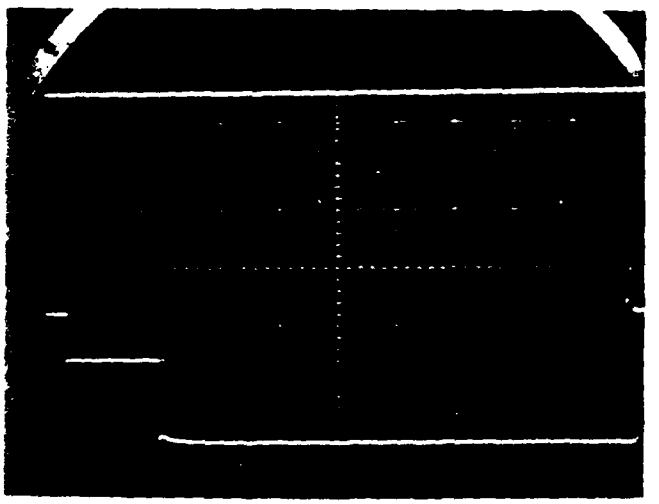
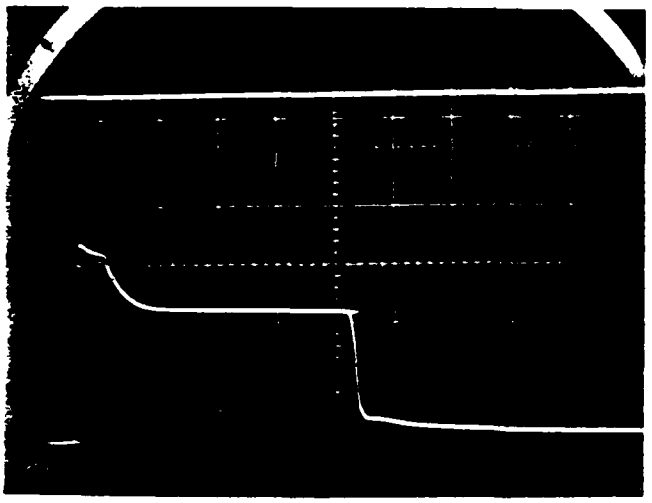


Figure 16b. Simulated "Stuck-on" Fault 1 ms Turn on Pulse Short Acrosss the Power Output Transistor to Simulate Fault

BIT RESPONSE TEST SERIAL #83 1/2A



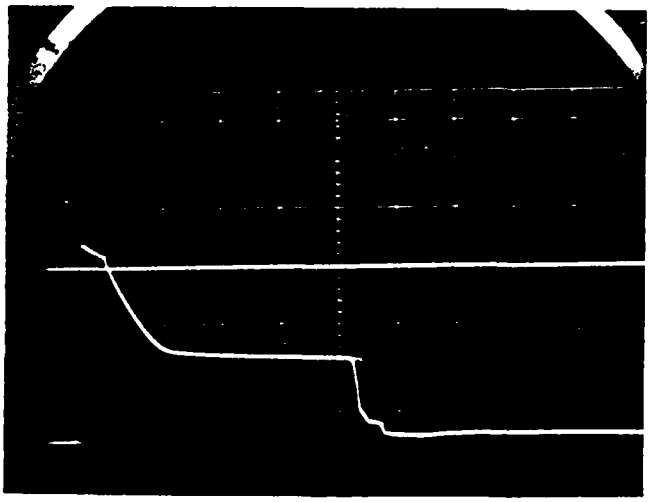
30V

OUTPUT VOLTAGE
10V/DIV

CONTROL INPUT
5V/DIV.

Horz. = 10μ Sec/DIV

Figure 16c. Simulated "Stuck On" Fault
BIT Response Sampled With
50 μ sec. Interrogation Pulse



30V

OUTPUT VOLTAGE
10V/DIV

CONTROL INPUT
5V/DIV

Horz. = 10μ Sec/DIV

Figure 16d. Normal Operation With 50μs
Interrogation Pulse

4.4.5 Problems Encountered During Testing

Some of the controllers being manufactured failed during testing or were determined to have an electrical parameter outside the specification limits. If the malfunction occurred during the final test, the unit's cover was removed and, if necessary, the hybrid substrates were taken off so that the cause of the fault could be determined.

When the first manufactured group of controllers was tested for Bit response time at 120°C, it was observed that some of the units would not have a stabilized Bit level within the allowed 50μ sec. Because some of the phototransistors were observed to have lag times of greater than 50 microseconds at 120°C, all the optocouplers on hand were tested for rapid response time characteristics at elevated temperature. Out of 369 parts tested, 237 had lag times of less than 40 microseconds. Since each of the 100 controllers require three optocouplers, an additional lot of optocouplers were purchased and tested.

Testing of the 10 and 5 Amp power assemblies indicated a greater voltage drop than anticipated across the output stage at rated load. This additional drop would cause an incorrect measurement of the controller output current by the sense circuitry. It

was determined that the additional drop occurred along the printed copper metal conductor trace. A copper ribbon in parallel to the conductor was added to reduce the drop to an acceptable level.

Three of the 2A controllers failed to turn on after the 600V short-term transient was applied across the power input and ground terminals. A visual examination of the assembled controllers did not reveal damage to the power or amplifier substrates, but close examination of the logic hybrid uncovered blown ground metallization on at least one of the three CMOS IC chips on each controller. This type of failure will usually manifest itself if the maximum specified CMOS operating voltage is exceeded. Since the controller design contained circuitry to prevent overvoltage on the internal supply rail, those components that should clamp or suppress transient spikes were suspected as being defective.

Two Zener diodes located on the power hybrid were incorporated so as to clamp the input spikes to a maximum 80 volt level which can safely be further reduced internally. Further testing revealed that due to the slow response of some of these diodes, spikes of up to 120 volts were being passed to the system. This fact in conjunction with the breakover of a protection diode located in the internal voltage regulator would pass a higher than allowable voltage onto the 12.5 volt supply rail. This then

resulted in the destruction of the CMOS devices. To correct the possible deficiency of the Zener diode response time, a 0.1 microfarad capacitor was added between power input and ground to absorb the initial surge until the Zener takes effect.

A few 5 amp. controllers failed preliminary testing by producing oscillations on the power output line during the turn on and turn off transitions. An examination of the test bench set-up revealed a poor power ground system. After correcting this deficiency, all but one of the units operated correctly during the rise and fall time period. The sixth unit was diagnosed to have a defective component in the closed loop circuitry that produces the transition period slopes.

During the production and testing, seven controllers encountered catastrophic failures during trip time tests. When these units were tested with a short between the output lead and ground in accordance with the specification, the controllers would not trip out in less than 1 millisecond as required, but would stay on for a longer duration until the sense resistor, acting as a fail-safe fuse would blow out. When the power decks of these units were examined, it was found that in addition to having an open sense resistor, the main power transistor had cratered under the emitter contact lead. The cause of this type of failure could be due to the control circuitry keeping the power stage on for too long during the overcurrent condition, thus, causing secondary breakdown, or because of premature secondary breakdown due to a weak

pass transistor in the power stage latching the output on even though the control to turn on had been removed.

Some of the failures were caused by the control circuitry keeping the pass stage on for too long until the designed energy limit of the transistor was exceeded. This was attributed to problems in the test equipment resetting the control circuitry.

Examination of the pulse generator signal that develops the input to turn the controller on indicated that some switch bounce from the pushbutton actuator was being passed through the system. This had the effect of resetting the trip out period and then turning the controller back on before the controller could normally trip out. This allowed the controller to be turned on for a longer accumulated period than intended between trip out times. The transistor would then short from emitter to collector due to secondary breakdown and would remain on until the sense resistor would blow open.

Although it was observed that at least one unit had failed due to the double pulse cause, it is certain that an additional unit failed due to other reasons. To prevent double pulses in the future, an additional circuit was built into the test set-up that would turn the controller on for a 20-second period.

It was determined that the remaining damaged power decks did not fail because of faulty external operation, but due to voids

under the transistor formed during assembly. These voids would cause hot spots on the transistor surface that would account for the premature breakdown. X-ray photographs were taken of the damaged power decks to examine the transistor contact area. In a few cases, the drive transistor and not the pass transistor had the high void concentration. Since it was observed that the pass stage sustained the damage, it is presumed that the driver prematurely broke down, thus, turning on the pass unit for too long until it, too, broke down and, then, shorted until the sense resistor opened.

5.0 RECOMMENDATIONS

The difficulties involved in producing 100 controllers point out the areas that could be improved on to ease manufacturing for large quantity production. Testing the controllers to meet the specification also indicated parameters that would be advantageous to change to produce lower cost power controllers. It is therefore recommended that the following modifications be incorporated into a controller specification for building production quantities.

Increase the control input current from the nominal 10ma value to at least 15ma. This will ease the selection among the few opto-couplers that operate at 120°C. Another benefit of a higher input control current is that the internal biasing resistances of the control circuit may be decreased which will decrease the Bit response settling time.

It is suggested that the mechanical specification require that one of the glass feed through insulators on the header be a differenct colored glass for indexing.

If the minimum current detection range for a fault could be defined to be approximately 15% of rated current with a tolerance of plus or minus 7% of the rated current level, then the precision of the internal voltage supply and reference voltages could be reduced.

It is also suggested that the additional items be specified and tested for future qualification:

Voltage drop from Pwr In to Pwr Out at over current levels.

The allowable output spike when power is initially applied to the Pwr In terminal.

Minimum voltage operation.

That the Fault Bit response will over-ride Trip when the voltage is removed from the Pwr In terminal.

APPENDIX A

PARTS LIST

HA01 POWER HYBRID PARTS LIST

	10A	5A	2A	1/2A
R24	100	200	500-1K	1K-2K
R25	130	130	130	130
R26	500	800	2K	4K
R27	.08 ohm	.08	.10	.40
R28	50	50		
R29	.08 ohm	.08		
R30	50	50		
R31	.08 ohm			
R32	50			
R33	.08 ohm			
R34	50			
R64	8	16	50	300-510
R65	1K	1K	1K	1K
R66	1K	1K		
R67	1K			
R68	1K			
D4	1N4148	1N4148	1N4148	1N4148
D6	1N3040B	1N3040B	1N3040B	1N3040B
D7	1N3040B	1N3040B	1N3040B	1N3040B
Q3	2N6316	2N6316	2N6316	2N6316
Q4	2N3019	2N3019	2N3019	2N3019
Q5	2N6316	2N6316	2N6316	2N6316
Q6	2N5339	2N5339	2N5339	2N5339
Q7	RCA 67654	RCA 67654	RCA 67654	RCA 67654
Q8	2N3792	2N3792	2N3792	2N3792
Q9	RCA 67654	RCA 67654		
Q10	2N3792	2N3792		
Q11	RCA 67654			
Q12	2N3792			
Q13	RCA 67654			
Q14	2N3792			
CK	.1 uF	.1 uF	.1 uF	.1 uF

HB01A LOGIC HYBRID PARTS LIST

R1	100 K Untrimmed
R2	560
R3	820
R4	13 K
R5	15 K
R6	200
R7	410
R8	20 K
R9	3.9 K
R10	3.9 K
R11	250 K
R13	1.8 M
R16	510 K
R17	510 K
R18	90 K
R55	13 K } Active Trim
R56	17.5 } Active Trim
R57	2.7 K
R58	7.5 K
R69	680
C1	1000 pF
C2	4700 pF
C3	0.01 μ
C7	1000 p
C9	0.01 μ
C10	0.01 μ
D1	MCC3.6A
D5	MZ43B10
D8	1N4148
D9	1N467
D2	1N4148
U1	CD4070BH (TA6950)
U2	CD4001BH
U3	CD4011BH
U7	LM723H
Q1	2N5550
Q2	2N5550
Q15	2N5550
Q16	2N2484
Q17	2N3251
Q18	2N2484
Q19	2N3019
Q20	2N5550
Q21	2N5550
Q22	2N5550

HB02 AMPLIFIER HYBRID PARTS LIST

R14	92 K
R15	47 K Active Trim
R19	75 K
R35	15 K
R36	56 K
R37	15 K
R38	15 K
R39	100 K
R41	465 K
R42	476 K
R44	20 K
R45	63 K
R46	8.1 K
R47	8.8 K
R48	46 K
R49	4 K
R50	15 K
R51	410 K
R52	406 K
R53	92 K
R54	47 K Active Trim
R61	820
R62	3.3 K
R63	1.2 M
C4	1000 p
C5	0.1 μ
C6	0.1 μ
C8	0.01 μ
U5	CA324H
U6	CA339H

D C CONTROLLER PARTS LIST

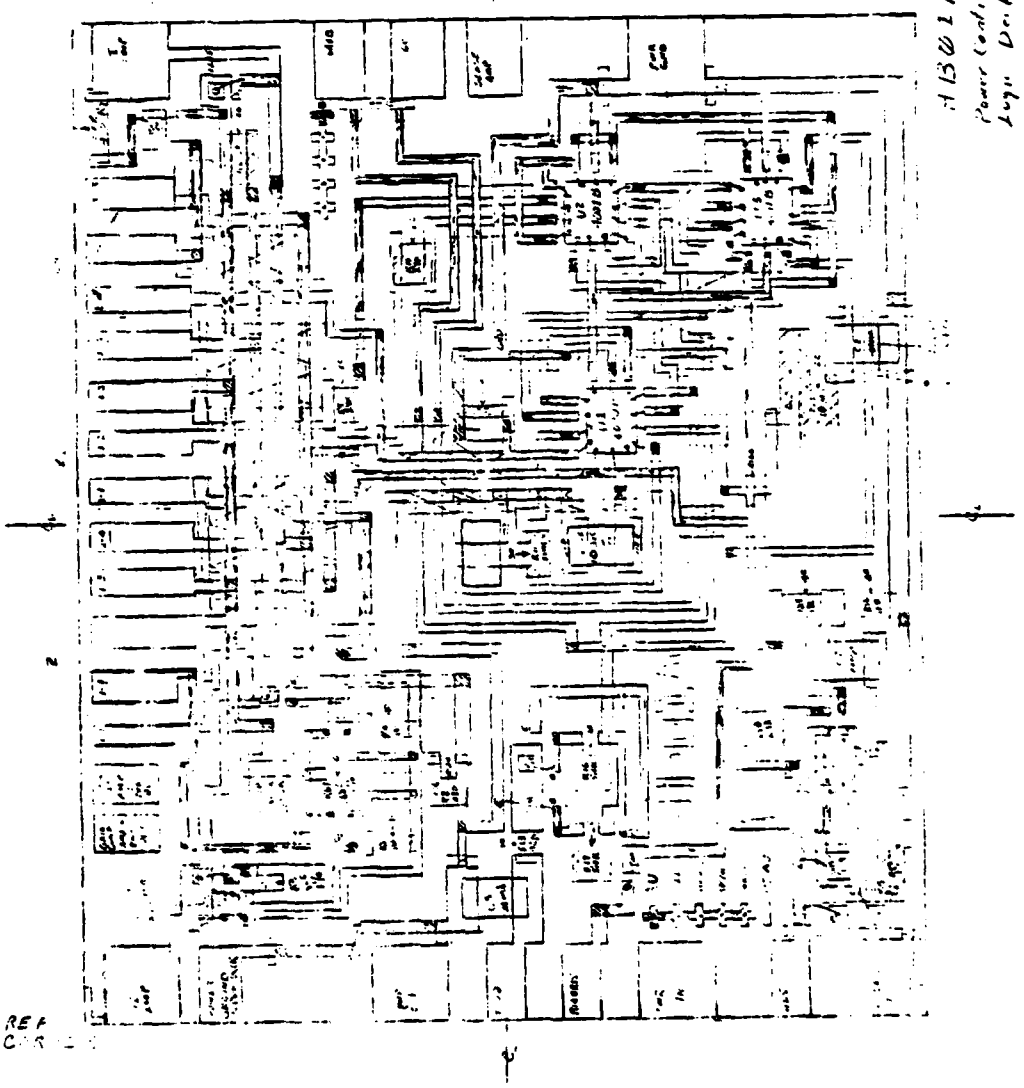
Header/Power Hybrid (HA01) subassembly
Logic Hybrid (HB01A)
Amplifier Hybrid (HB02)

Z1	OPI1991
Z2	OPI1991
Z3	OPI1991
D3	1N4002

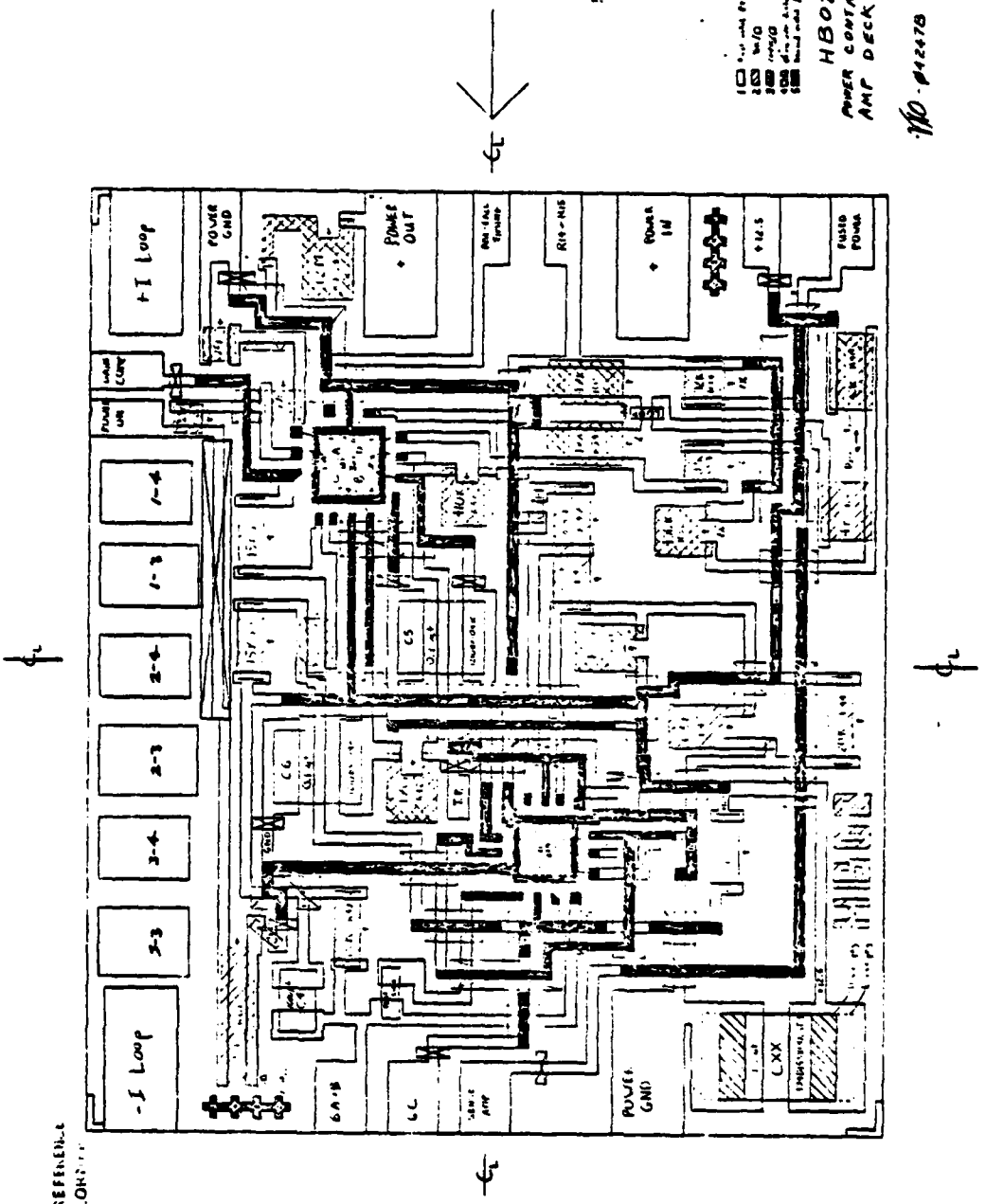
Header Cover

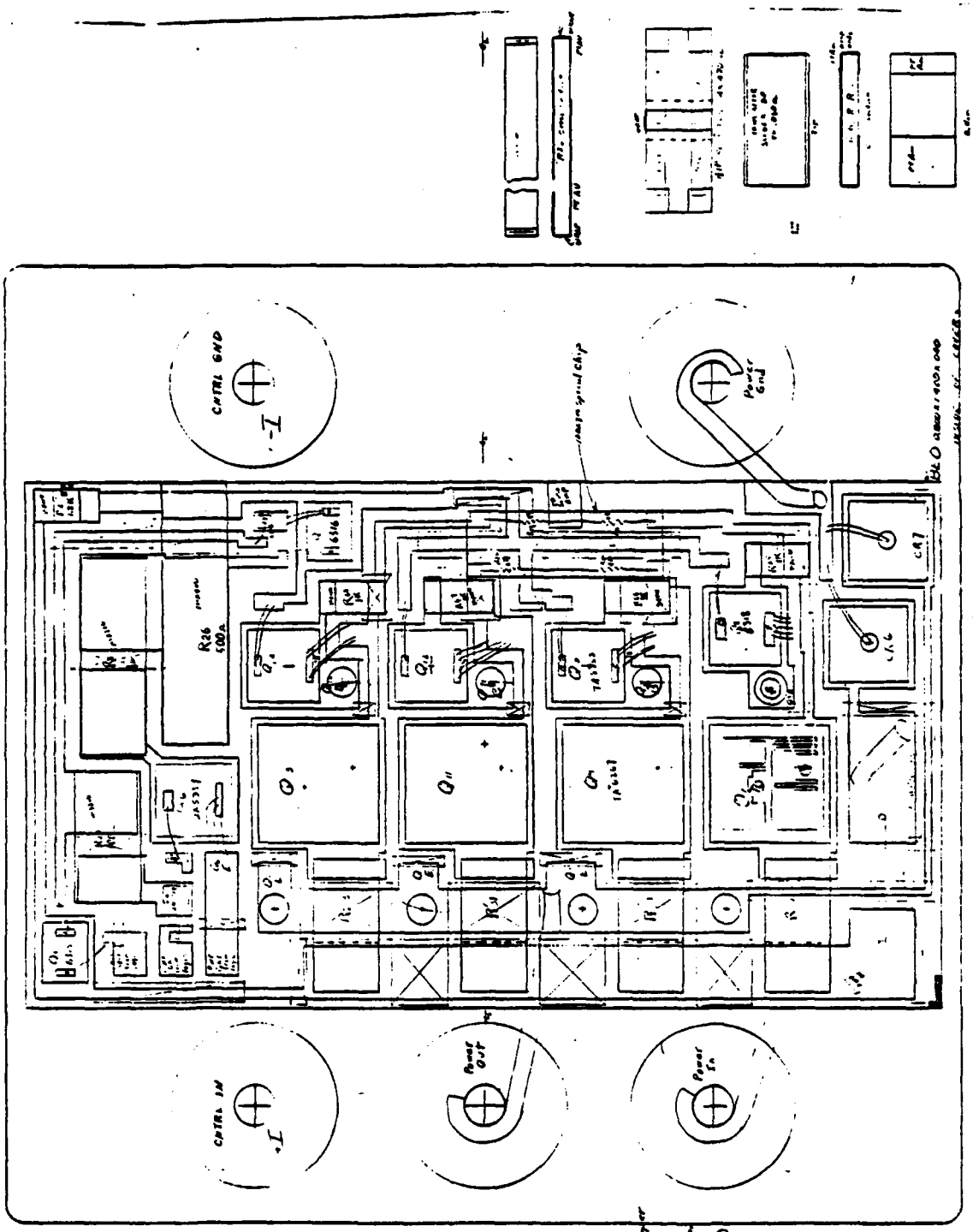
APPENDIX B

HYBRID LAYOUTS



A13014
Power Controller
Logic Deck





HA-01

APPENDIX C
TEST PROCEDURE

DC CONTROLLER ATP

LINE #/SERIAL #_____

CURRENT RATING _____ AMP

	LIMIT	DATA	COMPLY
1. Verify that the controller meets the physical requirements dictated by the specification and specification data sheet. EXTERNAL VISUAL AND MECHANICAL EXAMINATION 3.5/4.8.1			_____
2. Verify that the controller meets the solderability requirements of MIL-STD-202. SOLDERABILITY 3.7/4.8.3			_____
3. Verify that the controller has passed MIL-STD-202B, method 112B, condition C and procedure III-A, with an additional pressure cycle for fine leak detection and condition D for gross and leak detection. SEAL 3.8/4.8.4.2			_____
4. Connect the 5 controller terminals together and attach the AC High-Pot tester to the controller case and common terminal wire. Enable the high voltage output and increase the output level to 1000V RMS. Observe that there is no breakover during the 1 minute test period. **CAUTION - 1000V AC. DI-ELECTRIC WITHSTANDING VOLTAGE 3.9/4.8.5.1			_____
Decrease output level and turn off tester.			
5. Connect the five red test clips from the 100V leakage current set up to each one of the controller terminals. Attach the two black test clips to the controller case. Turn on the 100V supply and record the leakage current from the microammeter after 2 minutes. INSULATION RESISTANCE 3.10/4.8.6			_____
$= \frac{V_{TEST}}{I_{LEAK}}$ @ V_{TEST} = 100V	>100 MΩ	I_{LEAK} ____ μa	_____

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6. Turn off the supply and disconnect the two control terminal clip leads. Reconnect the two leads to the PWR OUT and PWR GND terminals. Disconnect the two case clip leads and reconnect them to the CTL^{IN} and CTL GND terminals. Turn on the 100V supply and record the leakage current after 2 minutes.

ISOLATION 3.11.4/4.8.7.4/4.8.6

V_{TEST} @ V_{TEST} = 100V	
I_{LEAK}	> 100 MΩ
I_{LEAK} < 1 μa	I_{LEAK} ____μa

Turn off the supply and remove all lead wires.

7. Connect the appropriate load for 100% of rated controller current to the load board. The load configuration can be obtained from the load board configuration matrix in the controller test setup procedure. Connect the load ammeter terminals so that rated current may be monitored.

   - Attach the controller to the heat sink fixture.
   - Solder the PWR IN and PWR OUT leads to the controller terminals. Attach the test monitor clips to all terminals.
   - Set the test switch to Normal and the control switch to Off.
   - Set the DVM function switch to volts.
   - Turn on the 30V and 17V power supplies and note that there is no load current.

   Switch the test point selector (TPS) to "A", and record DVM reading.

$V_{PWR\ IN}$ ____V

	LIMIT	DATA	COMPLY
8. Switch the control switch to ON and adjust the power supply so that $V_{PWR\ IN}$ equals 30V when $I_{PWR\ OUT}$ equals rated current as measured with the load. LOAD CONDITIONS DURING TEST 4.4.2/6.5.12	$V_{PWR\ IN}$ = 30.0V $I_{PWR\ OUT}$ = RATED	____V ____A	
9. Adjust the control current to 10.0 ma. Set the control switch to PULSE GEN. and enable the pulse generator. Adjust the pulse width and frequency so that the on time and off time are both 10 msec, as observed on the oscilloscope. Verify proper output operation for 2 minutes. CONDITIONING (RUN-IN) 3.6/4.8.2			_____
10. Set the time interval selector (TIS) to 1 and record reading from the interval timer (IT) + .01 msec. TURN ON DELAY 3.11.27/4.8.7.27/6.5.29	.1 to 1.0 msec	t_d ___ msec	_____
11. Set TIS to 2 and record IT reading. TURN ON TIME 3.11.2/4.8.7.2/6.5.14	.1 to 1.5 msec	t_{ON} ___ msec	_____
12. Set TIS to 3 and record IT reading. RISE TIME 3.11.3/4.8.7.3/6.5.16	.1 to .5 msec	t_r ___ msec	_____
13. Set TIS to 4 and record IT reading. FALL TIME 3.11.3/4.8.7.3/6.5.17	.1 to 2.0 msec	t_f ___ msec	_____
14. Set TIS to 5 and record IT reading TURN OFF TIME 3.11.2/4.8.7.2/6.5.15	<2.2 msec	t_{OFF} ___ msec	_____
15. Set the control switch to ON. Decrease the loop current to the point where $I_{PWR\ OUT}$ = 0, and record loop current. TURN OFF SIGNAL 3.11.1/4.8.7.12/6.5.11	>.4 ma	I_{CTL} ___ ma	_____

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	LIMIT	DATA	COMPLY
16. Increase the loop current to the point where $I_{PWR\ OUT}$ is at rated value and record loop current. TURN ON SIGNAL 3.11.1/4.8.7.1.1/6.5.10	< 9 ma	I_{CTL} ___ ma	_____
17. Increase the loop current so that I_{CTL} equals 10.0 ma. Set the TPS to "D" and record the DVM reading. CONTROL INPUT SIGNAL (NORMAL) 3.11.5/6.5.30.3	6.48 to 7.93V	V_{CTL} ___ V	_____
18. Set the control switch to PULSE GEN. and measure on the oscilloscope the control voltage response time for V_{CTL} to settle within the above range from the start of the pulse. CONTROL INPUT SIGNAL (NORMAL) 3.11.5/6.5.30.3	< 45 µsec	t_{BIT} ___ µs	_____
19. Set the control switch to ON. Turn the TPS to "C" and record the DVM reading. VOLTAGE DROP 3.11.6/4.8.7.6	≤ 1.05V	V_{DROP} ___ V	_____
20. With the clip-on current probe, measure the ground return current.		I_{GND} ___ ma	
Calculate the ON state power dissipation POWER DISSIPATION (ON STATE) 3.11.8/4.8.7.8 $(V_{DROP} \times I_{PWR\ OUT}) + (V_{PWR\ IN} \times I_{GND})$	1.1W for 1/2A 3.5W for 2A 8.5W for 5A 16.0W for 10A	P_{ON} ___ W	_____

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7/7/79

	LIMIT	DATA	COMPLY
21. Set the control switch to OFF. Switch to "A" to measure $V_{PWR\ IN}$. Measure GND current (= input current) with clip-on probe. Calculate the off state pwr disp = $(V_{PWR\ ON}) \times (I_{GND})$.		$V_{PWR\ IN}$ ____V I_{GND} ____ma P_{OFF} ____W	_____
POWER DISSIPATION (OFF STATE) 3.11.8/4.8.7.8	<.5W		
Disconnect load resistors. Switch test point selector to "B" and measure the voltage developed by the leakage current.	<.5V		
*** DO NOT PROCEED UNLESS THE ABOVE CONDITION HAS BEEN MET.			
22. Switch the DVM to read DC current on the lowest scale. Record the leakage current. LEAKAGE CURRENT 3.11.7/4.8.7.7	<8 μs for 10A <4 μa ALL OTHERS	I_{LEAK} ____μa	_____
23. Set the TIS to 6. Short out the load current ammeter and set up the current probe to monitor load current on the oscilloscope channel B. Set the pulse generator to EXT trigger position and the output to COMPLEMENT. Set the control switch to PULSE GEN. Observe a rated current indication on the scope.			_____
24. Adjust load for 150% rated output current. Press the manual switch on the pulse generator and record the 150% trip time from the IT. TRIP TIME 3.11.10/4.8.7.10(a)/ 6.5.8/6.5.24	1.3 to 8.2 sec	$t_{trip\ 150}$ ____sec	_____
25. Adjust load for 500% rated current. Press the manual switch to reset the controller and record the 500% trip time from the IT.	70 to 350 msec	$t_{trip\ 500}$ ____msec	_____

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	LIMIT	DATA	COMPLY
26. Adjust load for 850% rated current and record the 850% trip time when the controller is reset.	25 to 120 msec	$t_{trip\ 850}$ ___ msec	_____
27. Short out the resistive load and observe the $V_{PWR\ OUT}$ trace on the scope when the controller is reset by pressing the manual switch. Record the pulse width. TRIP TIME 3.11.10/4.8.7.10(a)(2)	<1 msec	$t_{trip\ SHORT}$ ___ msec	_____
28. Note that $V_{PWR\ OUT}$ remains at 0V after the controller trips out. RESET 3.11.12/4.8.7.12 TRIP-FREE CHARACTERISTIC 3.11.17/4.8.7.17			_____
29. Remove the load short and reset the controller. Observe that the controller turns on and trips out with the 850% trip time. This indicates proper operation after testing for rupture capacity. RUPTURE CAPACITY 3.11.11/4.8.7.10			_____
30. Reconnect the Channel B test box output to the scope. Switch the scope to negative trigger. Decrease the pulse generator pulse width to the 20K-2K range and the vernier to minimum. Increase the pulse width control so that the control signal off time is observed to be 4.5 msec when the manual switch is depressed. Note that the controller does not turn on by observing the load voltage response on the scope Channel A. RESET TIME 3.11.13/3.11.13.2/4.8.7.13/6.5.23			_____

4/12/77 JCM

AD-A082 759 RCA GOVERNMENT COMMUNICATIONS SYSTEMS CAMDEN NJ F/G 9/5
POWER CONTROLLER 28VDC LOAD SWITCHING (N.O. SPST).(U)
JAN 80 J B MCMACKIN N62269-77-C-0413
UNCLASSIFIED NADC -76125-30 NL

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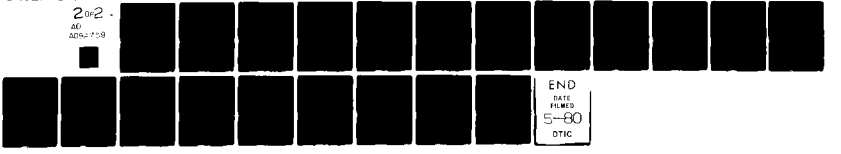
AD82 759



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	LIMIT	DATA	COMPLY
31. Adjust the loop current so that I_{CTL} equals 10.0 ma. Set the TPS to "D" and record the DVM reading. CONTROL INPUT SIGNAL (TRIP) 3.11.5/6.5.30.2 TRIP INDICATION SIGNAL 3.11.14/4.8.7.14	3.78 to 4.62V	V_{CTL} ___V	_____
32. Remove ammeter shunt. Reconnect the load for rated output current. Switch the control switch to ON and the DVM to AC volts. Set the TPS to "C" and read the AC ripple voltage generated by the controller ripple current. RIPPLE CURRENT 3.11.16/4.8.7.16/6.5.28	<.9V	V_{AC} ___V_{RMS}	_____
33. Switch the test switch to COMMON MODE and the TPS to E. Adjust the signal generator frequency to the lowest frequency scale and the amplitude control for 10V AC as monitored on the DVM. Sweep the signal generator up to 100 kHz while monitoring the load voltage on the scope. Adjust the signal generator output to maintain the 10V AC level as needed. Note that the load voltage remains constant. Set the control switch to off and sweep the signal generator to its lowest frequency and note that the output remains low. COMMON MODE REJECTION 3.11.25/4.8.7.25			_____
34. Set the DVM to monitor DC volts and the TPS to D. Set the test switch to NORMAL and adjust the load for 10% rated load current when the control switch is ON. Increase the loop current until either the BIT voltage is 15.0V and indicated on the DVM or the loop current is 15.0 ma. After 10 minutes reduce the loop current to 10.0 ma MAXIMUM CONTROL SIGNAL 3.11.28/4.8.7.25			_____

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	LIMIT	DATA	COMPLY
35. Record the BIT voltage from the DVM CONTROL INPUT SIGNAL (FAULT) 3.11.5/6.5.30.1	9.9 to 12.1 V	V_{CTL}____	_____
Set the pulse generator to SYNC trigger and the output to COMPLEMENT. Set the control switch to PULSE GEN and adjust the pulse width so that the on time and off time are both 10 msec. as observed on the oscilloscope.			
36. Set the TIS to 3 and record the IT reading for rise time.	0.1 to 0.5 msec	t_r____msec	_____
Confirm that the above rise time is the same as that recorded in step 12.	tr of #12 ±0.05 ms		_____
Set the pulse generator to EXT.			
37. Increase the load current up to the controller's rated value and note that the NORMAL BIT level returns.			
BIT FAULT INDICATION SIGNAL 3.11.29/4.8.7.29(a)	6.48 to 7.93 V	V_{CTL}____ V	_____
38. Turn the TPS to C and record the DVM reading.	<1.05 V	V_{DROP}____ V	_____
Confirm that the above voltage drop is the same as that recorded in step 19.	V_{DROP} of #19 ±0.05 V		_____
39. Turn the TPS to D. Turn off the 30V power supply and note the FAULT BIT voltage BIT FAULT INDICATION SIGNAL 3.11.29/4.8.7.29(b)	9.9 to 12.1 V	V_{CTL}____ V	_____
40. Set the pulse generator to SYNC. Measure the control voltage response time for V_{CTL} (on channel B) to settle within the above range from the start of the pulse.			
CONTROL INPUT SIGNAL (FAULT) 3.11.5/6.5.30.3	<45 µs	t_{BIT}____ µs	_____
Set the control switch to OFF before removing the test leads.			

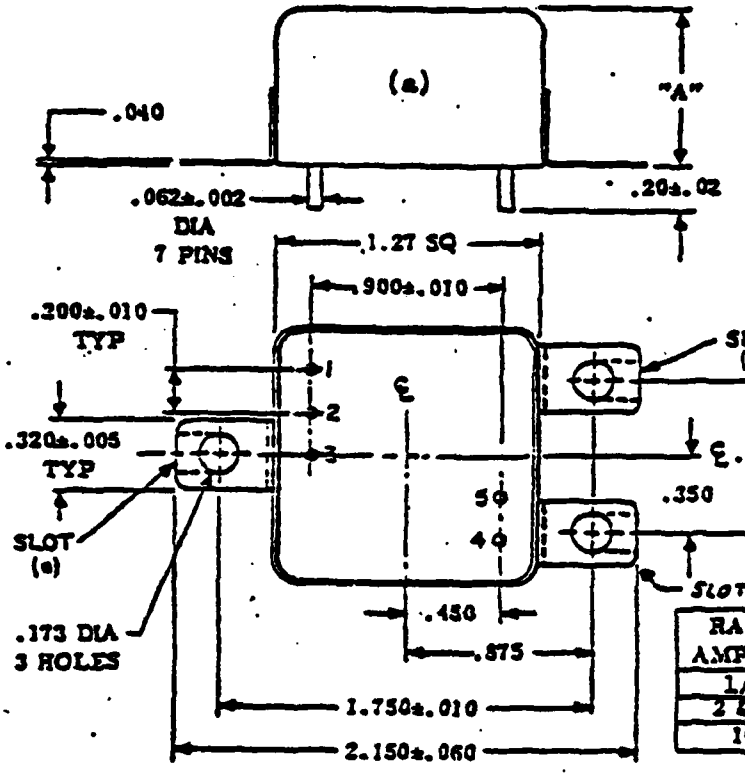
6/14/79 JBM

APPENDIX D
SPECIFICATION

MILITARY SPECIFICATION SHEET

POWER CONTROLLER, DC LOAD SWITCHING
SPST, NORMAL OPEN, ½ THRU 10 AMPERES

The complete requirements for procuring the controllers described herein shall consist of this document and the latest issue of



PIN NO.	IDENTIFICATION FUNCTION
1	Power In
2	Power Out
3	Power Ground
4	Control
5	Signal Ground

(b)

RATING AMPERES	"A" MAX	WEIGHT
1/2	.50	2.0 OZ
2 & 5	.75	2.5 OZ
10	1.0	3.0 OZ

NOTES:
(a) Name plate location.
(b) Pin designations are for reference only and do not appear on header.
(c) Terminals shall be tin plated followed by a flow process or coated with composition Sn 40 to Sn 70 solder conforming to QQ-S-571.
(d) TS7602/01-001, 002 & 003 only
(e) TS7602/01-001, & 002 only
(f) TS7602/01-001 only

EQUIREMENTS:

MECHANICAL AND DIMENSIONAL CHARACTERISTICS

Configuration	See Figure 1
Dimensions	Inches
Tolerances	±0.02 for two place decimals ±0.005 for three place decimals
Enclosure	Type 4
Weight	See Figure 1
Mounting torque	15 in. lb.
Terminal strength	
Pull test	Condition A - 10 pounds
Bend test	Condition C - 5 pounds
Leak rate	10^{-6} atm cc/sec.

THERMAL CHARACTERISTICS

Thermal resistance case-to-sink	0.50°C/watt with specified mounting torque
Heat sink temperature (design consideration)	See Table I

ELECTRIC CHARACTERISTICS (-54 to 120°C case temperature unless otherwise specified)

General

Circuit arrangement	SPST NO
Insulation resistance	100 megohms minimum
Dielectric withstanding voltage	Applicable
Isolation	Applicable
Life (operating cycles)	10^6 minimum
Radio interference	Applicable
Leakage current	See Table I
Power dissipation	
'ON'	See Table I
'OFF'	See Table I
Common mode rejection	Applicable

Power Circuit

Supply voltage	
Steady state	30 volts dc maximum 28 volts dc rated 17.5 volts dc minimum
Transient (long term)	80 volts dc maximum (50 ms) 9.5 volts dc minimum (50 ms)
Transients (short term)	±600 volts dc (10 mjoules max)

Current	
Rated (no load to 100% rated)	See Table I
Frequency (rated)	Not applicable
Voltage drop (no load to rated)	1.2 volts dc maximum @ -54°C .9 volt dc maximum @ 100°C
Current limiting	270-330% rated load
Ripple current	
(no load to 100% rated)	3% rated maximum
(in current limit to short circuit)	5% rated maximum
Rupture capacity	Unlimited
DC offset voltage	Not applicable
Let through current	
Amplitude	330% of rated current maximum
Time	10 milliseconds maximum
Fail safe	See Figure 1
Reset immunity	Not applicable
Transients	
Operating voltage	Applicable
Spike overvoltage	Applicable
Standby power	Not applicable
Response	
Turn on time	1.5 milliseconds maximum
Rise time	0.1 milliseconds minimum 0.5 milliseconds maximum
Turn off time	2.0 milliseconds maximum
Fall time	0.1 milliseconds minimum 2.0 milliseconds maximum
Turn on delay	0.1 milliseconds minimum 1.0 milliseconds maximum
Trip free	Applicable
Trip time	See Figure 1
Nonrepetitive reset	Applicable (30 seconds minimum between resets)
Repetitive reset	Applicable
Zero voltage turn on	Not applicable
Zero current turn off	Not applicable

Control Circuit

Supply voltage	15.0 volts dc maximum
Current	15.0 milliamperes maximum
Turn-on Current	10.0 milliamperes rated 9.0 milliamperes minimum
Turn-off Current	1.0 milliamperes maximum

Control Circuit (CONT)

BIT input impedances and signals (±10%)	
Fault	1.1k ohms, 11 Volts dc
Normal	720 ohms, 7.2 Volts dc
Trip	420 ohms, 4.2 Volts dc
Removal time to reset	5.0 milliseconds minimum 20.0 milliseconds maximum
Turn on voltage	Not applicable
Rate of change	Not applicable
Turn off voltage	Not applicable
Rate of change	Not applicable
Input transients	Applicable

Reset Circuit

Supply voltage	Not applicable
Reset voltage	Not applicable
Rate of change	Not applicable
Input transients	Not applicable
Application time to reset	Not applicable

ENVIRONMENTAL CHARACTERISTICS

Case temperature	
Operating	-54°C to 120°C
Storage (nonoperating)	-65°C to 150°C
Shock	
Mechanical	100 G for 11 milliseconds
Temperature	-54°C and 71°C
Vibration	Applicable
Acceleration	100 G
Salt fog	Applicable
Humidity	Applicable

Operation at temp. extremes . . . . . Applicable
Temperature-altitude . . . . . Applicable
Operating ambient
Temperature . . . . . -54°C to 95°C
Altitude . . . . . Sea level to 100,000 feet

TABLE I. Dash numbers and applicable characteristics

Part No. TS7602/01	Current Rating (1) Amperes	Power Dissipation - Watts Max ON -54°C	ON 25°C	ON 100°C	OFF 100°C	Leakage Current-Max (Microamperes)	Heat Sink Temp °C Max.
001	0.5	1.3	1.1	1.0	.50	500	119
002	2.0	4.0	3.5	3.0	.50	500	118
003	5.0	9.0	8.5	8.0	.50	500	116
004	10.0	17.0	16.0	15.0	.50	1000	112

(1) Steady state

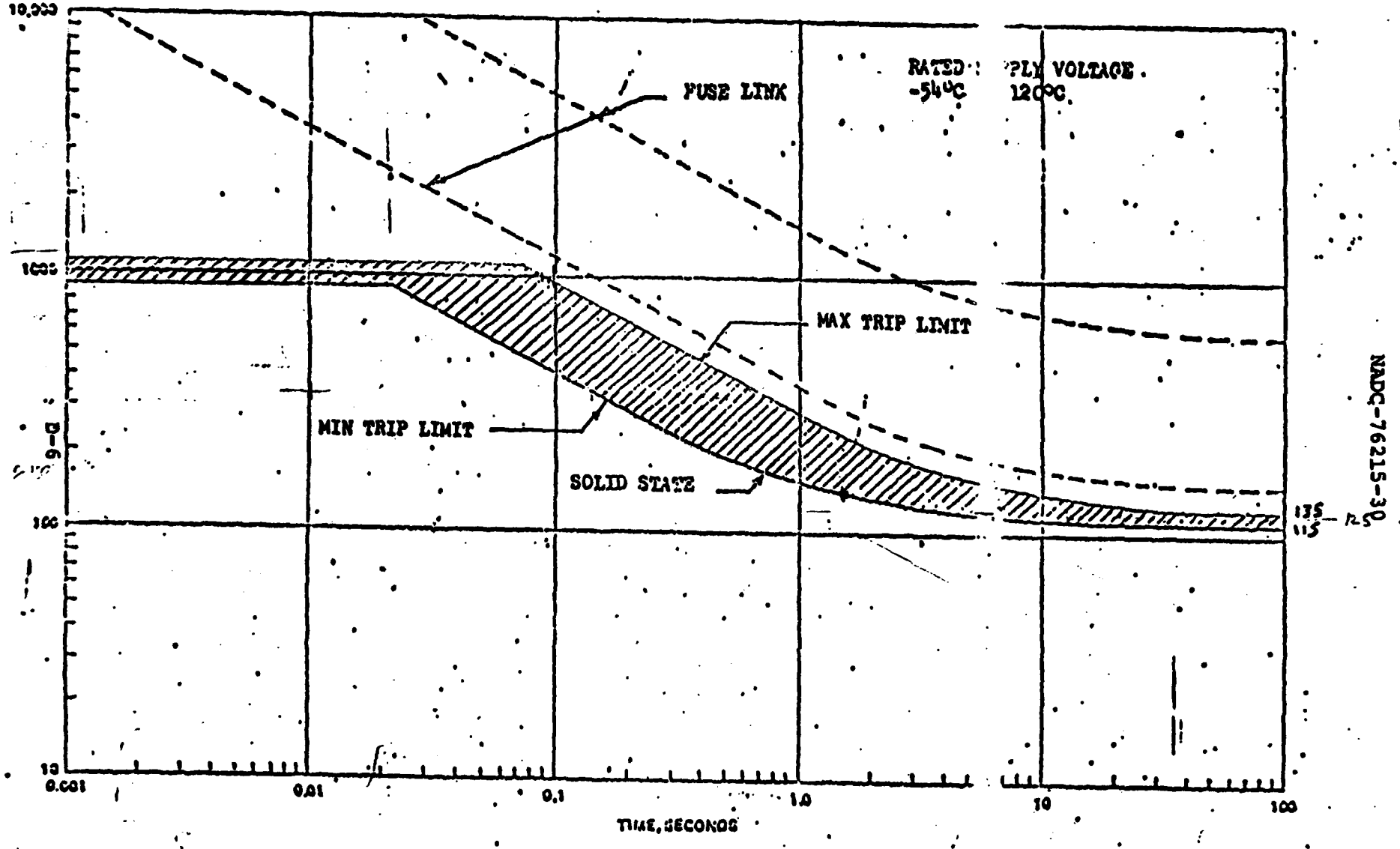


FIGURE 1 ALTERNATE TRIP CHARACTERISTICS

APPENDIX E

FAILURE MODE ANALYSIS

1.0 INTRODUCTION

This failure mode analysis has been prepared in response to Paragraph 7 of the Work Statement No. 30P9—Solid State Power Controllers, dated 6 April 1976. The analysis has been conducted in accordance with Paragraph 3.4.2 of the Reliability Program Plan for Power Controller DC, Load Switching, dated 15 October 1977. The design data basis for this analysis is the final design of the DCPC as presented elsewhere in this report.

2.0 FUNCTIONAL ANALYSIS

The failure mode analysis is derived from a functional analysis of the controller. The major functions of the controller with respect to the power input and output terminals are as follows:

The controller will:

1) Turn on within the specified rise time delay limits when commanded on.
2) Turn off within the specified fall time limit when commanded off.
3) Trip out within the specified time limits and will not trip out prematurely.
4) Maintain the Power-Input-to-Power-Output voltage drop below the specified limit.
5) Maintain the power dissipation below the specified limits.

6) Maintain current leakage at the Power Output below the specified limit when off.

7) Provide the specified current limiting.

8) Maintain correct operation (no trip out) after exposure to the specified long-term and short-term transient voltages at the Power Input.

The internal functions of the controller are identified and grouped into three major subfunctions as shown in the controller functional block diagrams of Figure 3 (Logic), Figure 5 (Amplifier) and Figure 8 (Power) in Section 2 (Circuit Design and Operation) of this report. These three major elements (plus a separate semiconductor diode) represent the physical partitioning of the controller into hybrids with interconnections as shown in Figure 1. The output signals (lines) from each hybrid or deck to the other two are the outputs whose failure modes and effects are analyzed and recorded in detail in this appendix.

3.0 FAILURE MODE ANALYSIS PROCEDURE

The output signal lines were grouped by major subfunction and analyzed one-by-one in terms of failure modes and effects. First, each output line was identified; then, the major possible failure modes were determined; the failure effects on the other two major subfunctions and on the controller power output were obtained; the symptom of failure, if any, presented to the controller input terminals wad deduced.

The conditions attendant on the analysis of each individual failure mode are as follows:

1) Only a single failure has occurred (the probability of a time overlap double failure occurrence is so low as to be negligible)

2) The controller has been thoroughly debugged and tested and is running normally (commanded on or off) just prior to failure.

3) The failure symptons recorded are those directly available to the external system observed as voltage levels at the control input of the controller; indirect symptoms such as the reaction of the controller-fed load equipment, and its subsystem and system are assumed not to be always available or to be ambiguous with respect to the location and cause of failure.

4) Control input terminal voltage levels are considered to provide Bit status information and fault symptoms; they do not provide a major function controller output.

4.0 ANALYSIS RESULTS

Failure modes and effects are documented on the FMEA (failure-modes-and-effects) Table E-1 attached:

1) Logic hybrid outputs: Sequence Nos. 1-3
2) Amplifier hybrid outputs: Sequence Nos. 4-8
3) Power hybrid outputs: Sequence Nos. 9-10

Several of these failure modes and their resultant effects were noted during debugging and testing of the one hundred controllers produced.

DC CONTROLLER

FAILURE MODES AND EFFECTS ANALYSIS

LOGIC DECK

SEQ. NO.	OUTPUT FUNCTIONAL DESCRIPTION	FAILURE MODE NO. & DESCRIPTION	POSSIBLE CAUSES	SYMPTOMS & DETECTABILITY	EFFECT OF FAILURE MODE	
					LOCAL EFFECT	END EFFECT
1	+12.5 V - Precision reference and supply output.	0V on internal supply line.	Q15 Open; Q19 Open; U7 Malfunction; C9 Short; C8 Short; D5	Condition A	Supply to the control circuitry removed. Power on amplifier (U5/A) cannot supply turn on signal to power switch.	Controller will not switch on. Therefore, no output delivered to load.
M-4		Low voltage on internal supply line.	Q15 Base open; U7 Malfunction; D5 Leaky.	Condition B or Condition A, depending on faulted supply voltage.	Reference level to voltage comparators on AMP hybrid lower thus lowering the threshold voltages for trip and minimum current detection.	Premature trip out of the controller.
		High voltage on internal supply line.	Q19 Base Open; D9 leaky; U7 Malfunction	Condition C	Reference level to voltage comparators increased, thus increasing threshold voltages for trip and minimum current detection. Possible damage to CMOS IC's.	Controller will not trip out. Output may be latched off or on, independent of the control input.
NOTE:	For description of symptom Conditions A through E, See Symptom Description List. Follow these FMEA worksheets.					

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TABLE E-1.

SEQ. NO.	OUTPUT FUNCTIONAL DESCRIPTION	FAILURE MODE NO. & DESCRIPTION	POSSIBLE CAUSES	SYMPTOMS & DETECTABILITY	EFFECT OF FAILURE MODE	
					LOCAL EFFECT	END EFFECT
2	Ref. Ramp. - Ref. Ramp to develop output rise and fall time.	Stuck off.	C3 shorted; Q17 Open, Q15 Open; U2/D Stuck High; Supply Ref. Stuck Low.	Condition A	Pwr. On amp. (U5/A) will not receive turn on signal.	Controller will not turn on.
		Stuck on.	Q17 shorted; U2/D Stuck low due to faulty logic.	Condition D or Condition E, depending on DCPC output current.	Pwr. On amp. receives constant turn on signal.	Controller will not turn off or trip out.
		Will not switch Completely high.	Poor gain Q17; Supply Ref. Low.	Condition A or Condition F, depending on REF RAMP voltage level.	Intermediate output to Pwr. On Amplifier.	Reduced voltage delivered to load.
3 [illegible] 5	Control Input Loop BIT Response indicates TRIP, NORMAL, or FAULT status when 10ma input applied.	BIT level lower than allowable levels for any BIT response.	D8 Leaky; D1 Open.	Response voltage outside of detection levels for all Controller states.		Improper Controller status detected on Control input terminals; Power Output unaffected.
		Invalid BIT fault condition detected (normal operation)	U2/B stuck high; U1/C stuck low; Z1 open; Q1 open.	FAULT BIT state indicated for steady state and under interrogation		Improper Controller status detected on Control input Terminals. Power Output unaffected
	Invalid BIT NORMAL condition detected (Trip condition)	U2/A stuck high Z2 open Q2 open	Control input terminals indicates NORMAL state.			Controller Power output is turned off when it should be on.

TABLE E-1.

SEQ. NO.	OUTPUT FUNCTIONAL DESCRIPTION	FAILURE MODE NO. & DESCRIPTION	POSSIBLE CAUSES	SYMPTOMS & DETECTABILITY	EFFECT OF FAILURE MODE	
					LOCAL EFFECT	END EFFECT
	=8V BIT level during trip state (correct level for TRIP is 4.2V)	Z1 open; Q1 open; U2/B stuck high; U1/C stuck low	BIT indicates invalid state, i.e. a voltage level in between a valid normal state voltage.			Controller Power Output is turned off when it should be on.
	Control Input (Cont.)	BIT levels higher than allowable levels for any BIT response.	C10 shorted	Control input terminal response voltage above normal state detection levels for all controller states.		a. Controller may not turn on at low temperature. b. Controller, if tripped out, may turn itself back on.
		BIT level above 12V.	Z3 open; Q20 open.	Higher than allowable level for FAULT state. FAULT condition may not be detected.	Turn on control signal will not reach control logic.	Controller will not turn on—no output delivered to load.
4	Supply Ref. - signal level proportional to Power Input Voltage	Level shorted to ground.	U5/D shorted.	Condition A.	Q17 input voltage too low.	Controller will not turn on.
		High supply Ref. value.	Input to U5/D leaky.	No symptom at control input terminals.	None.	Power Output rise/fall time out of spec. Short rise times; long fall times during turn on and turn off of controller output.
5	TRIP-signal to control logic indicates trip condition has occurred	Stuck high.	C4 shorted; U6/B on U6/A output open; C6 shorted; U5/D Malfunction	Condition G	Solid state switch will not turn off during over current conditions.	Controller will not trip out. Possible damage to the controller output stage and/or load.
		Stuck low.	U6/B or U6/A latched low; Q16 leaky from C to B; Sense input open; (blown out sense resistor)	Condition H	Constant trip indication to control logic (even without load current)	Controller will not turn on.

TABLE E-1.

SEQ. NO.	OUTPUT FUNCTIONAL DESCRIPTION	FAILURE MODE NO. & DESCRIPTION	POSSIBLE CAUSES	SYMPTOMS & DETECTABILITY	EFFECT OF FAILURE MODE	
					LOCAL EFFECT	END EFFECT
6	$\overline{\text{MINI}}$ - signal to control logic indication >x15% rated load current.	Stuck high.	U6/C output open.	FAULT BIT indication when output is at rated current. NORMAL BIT indication with interrogation pulse.	Control logic will not receive indication of minimum current.	No effect on power output.
		Stuck low.	U6/C output shorted to ground. Q16 leaky from C to B.	FAULT BIT indication detected with interrogation pulse when there is no output current (power output commanded off.)	Control logic will receive constant minimum output current signal.	No effect on power output.
7	Gain Comp. provides additional drive to the power switch during overcurrent excursions of the load.	Gain Comp. stuck low.	U5/C output defective. U6/D stuck high.		No additional drive to power switch.	Current limiting of the Controller output during an overcurrent condition to the load will cause the output switch to absorb power, thus heating the power transistors and increasing their gain. This will reduce the voltage drop between the input and output terminals and will increase the effective current limiting level. This effect will become more predominate as the case temperature is lowered.
		Gain Comp. stuck high.	U5/C output defective U6/D stuck low.		Gain compensation always provided to power switch	High controller power dissipation when turned on.

TABLE E-1.

SEQ. NO.	OUTPUT FUNCTIONAL DESCRIPTION	FAILURE MODE NO. & DESCRIPTION	POSSIBLE CAUSES	SYMPTOMS & DETECTABILITY	EFFECT OF FAILURE MODE	
					LOCAL EFFECT	END EFFECT
8	Power On - signal from control circuitry to power switch to turn-on.	Stuck low.	U5/A output defective	Condition A; Condition H	Q4 of power switch cannot turn on.	Controller will not turn on.
	Power on.	Stuck high.	U5/A output defective	Condition D Condition G	Q4 always turned on thereby keeping the power switch turned on.	Controller will not turn off. Load and/or controller may be damaged if an overcurrent condition occurs.
9	Sense - Voltage referenced to the power input terminal that is linearly proportional to output current.	Open circuit.	Blown out sense resistor.	Condition H	Control circuitry sense overcurrent condition.	Controller will not turn on.
10	Power Out.	Stuck on (power switch stuck on)	Q7, Q9, Q11, Q13 shorted; Q8, Q10, Q12, Q14 leaky; Q4 shorted/leaky; Q6 shorted/leaky.	Condition D Condtion G	Same End Effect	Controller will not turn off. Load may be damaged if an overcurrent condition occurs.
		Stuck off.	Sense resistors blown open; Q4 open; Q6 open; Q8, Q10, Q12, Q14 open; Q7, Q9, Q11, Q13 open.	Condition A Condition H	Same as End Effect.	Controller turn on for multiple output stage units (10A or 5A) 1/2A or 2A controllers will not turn on.

TABLE E-1.

SEQ. NO.	OUTPUT FUNCTIONAL DESCRIPTION	FAILURE MODE NO. & DESCRIPTION	POSSIBLE CAUSES	SYMPTOMS & DETECTABILITY	EFFECT OF FAILURE MODE	
					LOCAL EFFECT	END EFFECT
	Power Out (cont'd.)	Output not switched fully on.	Burn out of one or more of the power switching transistors (Q7, Q9, Q11, Q13) or drive transistors	Voltage drop between Power Input and Output greater than 1.05 volts at room temperature.	High power dissipation concentrated in solid state switch.	Load voltage may be below acceptable levels. Possible output current limiting during overcurrent conditions. Voltage drop between Power Input and Output greater than 1.05 volts at room temperature.
		Leaky output when control signal removed.	Leaky power switching or drive transistor.	Control input terminal voltage may not indicate a FAULT state depending on the amount of leakage. If current is less than ≈15% of rated output fault will not be indicated.	Possible above normal power dissipation for off condition.	Out of spec leakage current delivered to load.

TABLE E-1.

TABLE E-1

SYMPTOM DESCRIPTION LIST

Condition A

Fault BIT state indicated at control input terminals during steady state application of input signal. Normal state indicated when input terminals are interrogated with 50μs pulse.

Condition B

Control input terminals will indicate a trip state. The input terminals may indicate a fault condition when interrogated with a 50μs pulse.

Condition C

If the +12.5V supply line voltage goes above 20V, the CMOS logic may be damaged, in which case, either symptom condition A or D may be evident. An increase in the 12.5V line voltage will cause a slufting up of the trip curve; therefore, the controller may not trip out during over current conditions. The increase of the threshold levels may also cause a steady state fault indication when the controller is passing current above the normal minimum current level (≈15%).

Condition D

Controller output will not switch off. Normal BIT state indicated when input signal applied. Fault state indicated when interrogation pulse applied.

Condition E

During over current condition, the trip current level is detected but control logic may be stuck so that trip BIT state is indicated but controller does not turn off.

Condition F

Solid State switch will not saturate; thus, the power output terminal voltage will be below normal. Depending on this voltage, the output current to the load may produce a Normal or a Fault BIT state.

Condition G

Controller will not trip out when an overcurrent condition exists. Normal BIT state indicated at input terminals.

Condition H

Controller will not turn on. BIT TRIP indication returned at steady state turn-on and during interrogation pulse.